

Compal Confidential

Schematics Document

Intel Huron River

Sandy Bridge with Cougar Point core logic

2010-10-27

REV:1.0

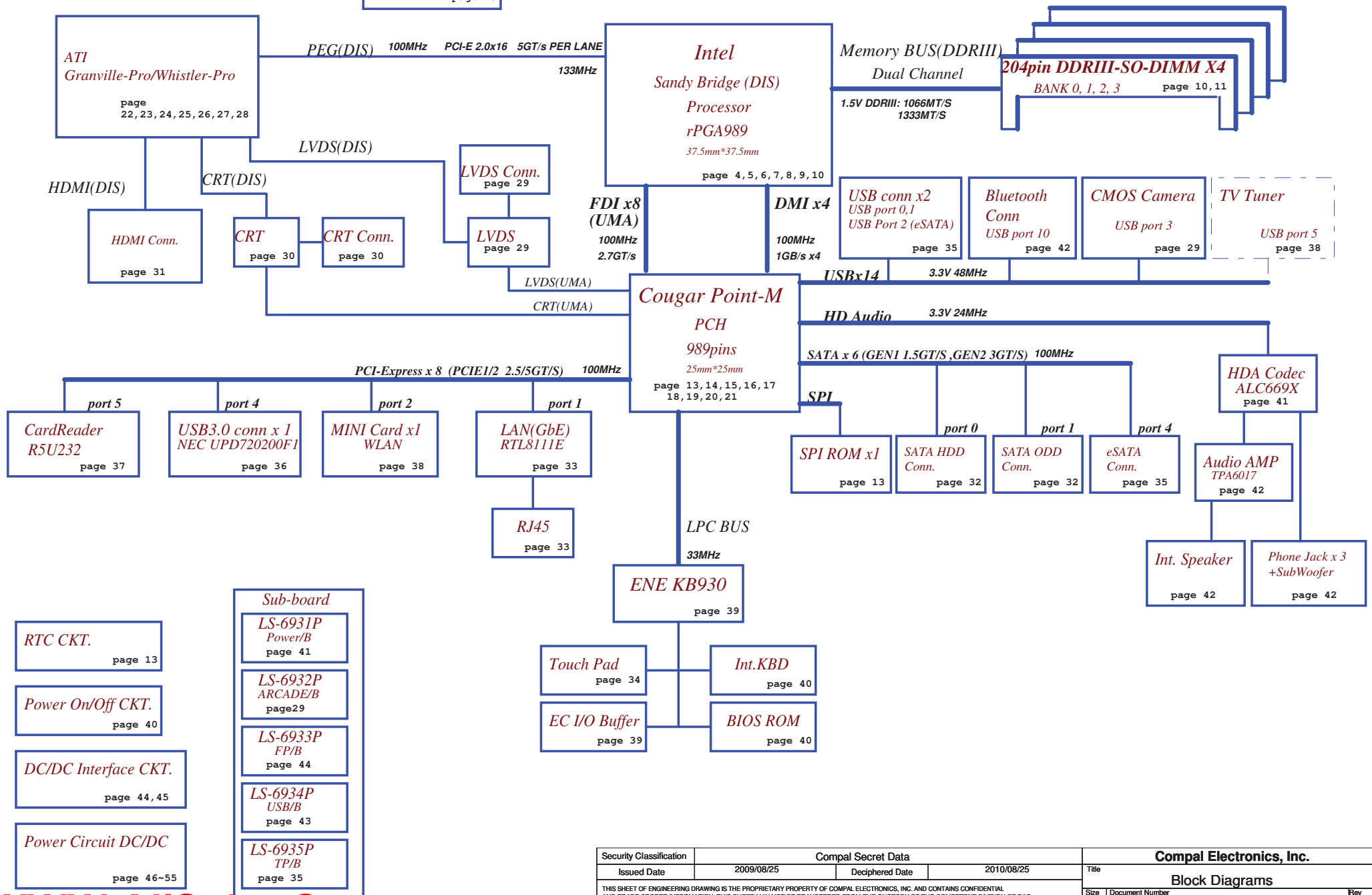
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Model Name : P5LM0

File Name : LA-6931P

Fan Control
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Voltage Rails

Power Plane	Description	S1	S3	S5	DGPU (DIS)	IGPU (SG)
VIN	Adapter power supply (19V)	N/A	N/A	N/A		
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A		
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A		
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF		
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF		
+1.05VS_VCCP	1.05V switched power rail for CPU (PCH)	ON	OFF	OFF		
+VGFX_CORE	Core voltage for IGPU	ON	OFF	OFF		
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF		
+1.5VS	1.5V switched power rail	ON	OFF	OFF		
+1.8VS	1.8V switched power rail	ON	OFF	OFF		
+3VALW	3.3V always on power rail	ON	ON	ON*		
+3VALW_PCH	3.3V power rail for PCH	ON	ON	ON*		
+LAN_JO	3.3V power rail for LAN	ON	ON	ON*		
+3VS	3.3V switched power rail	ON	OFF	OFF		
+5VALW	5V always on power rail	ON	ON	ON*		
+5VS	5V switched power rail	ON	OFF	OFF		
+VSB	VSB always on power rail	ON	ON	ON*		
+RTCVCC	RTC power	ON	ON	ON		
+VGA_CORE	5V power rail for GPU	ON	OFF	OFF	ON	OFF
+1.5VSDGPU	1.5V power rail for VRAM	ON	OFF	OFF	ON	OFF
+1.8VSDGPU	1.8V switched power rail for GPU	ON	OFF	OFF	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
--------	---------	--------	---------

Ibex SM Bus address

Device	Address
--------	---------

STATE	SIGNAL				SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON				
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW				
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF				
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF				
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF				

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
* 3	0.4
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
DIS Only	DIS@
Switchable Graphics	SG@
Granville	GRA@
Whistler	WHI@
For CIR	CIR@
USB2.0 bus	USB2@
DDR M1	M1@
DDR M3	M3@
For 45 level	45@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	USB/B
		1	USB Conn.
	UHCI1	2	
		3	
	UHCI2	4	Mini Card 1
		5	Mini Card 2
	UHCI3	6	
		7	
EHCI2	UHCI4	8	USB Conn.
		9	eSATA USB
	UHCI5	10	CMOS Camera
		11	Finger Print
	UHCI6	12	USB3.0 @
		13	Blue Tooth

43 Level BOM Config

Granville DIS: GRA@ DIS@ CIR@ M1@
Whistler SG: WHI@ SG@ CIR@ M1@

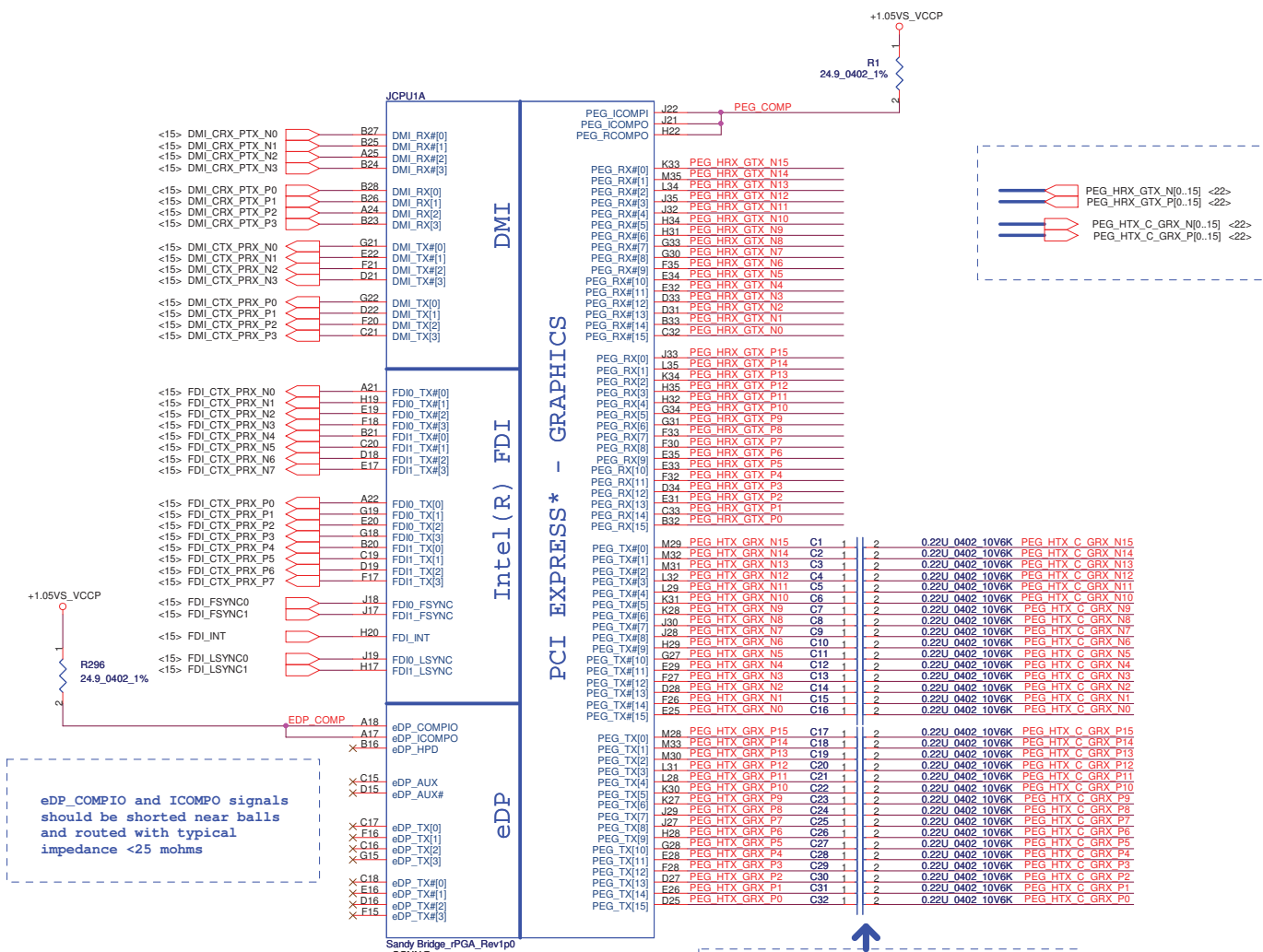
45 Level BOM Config

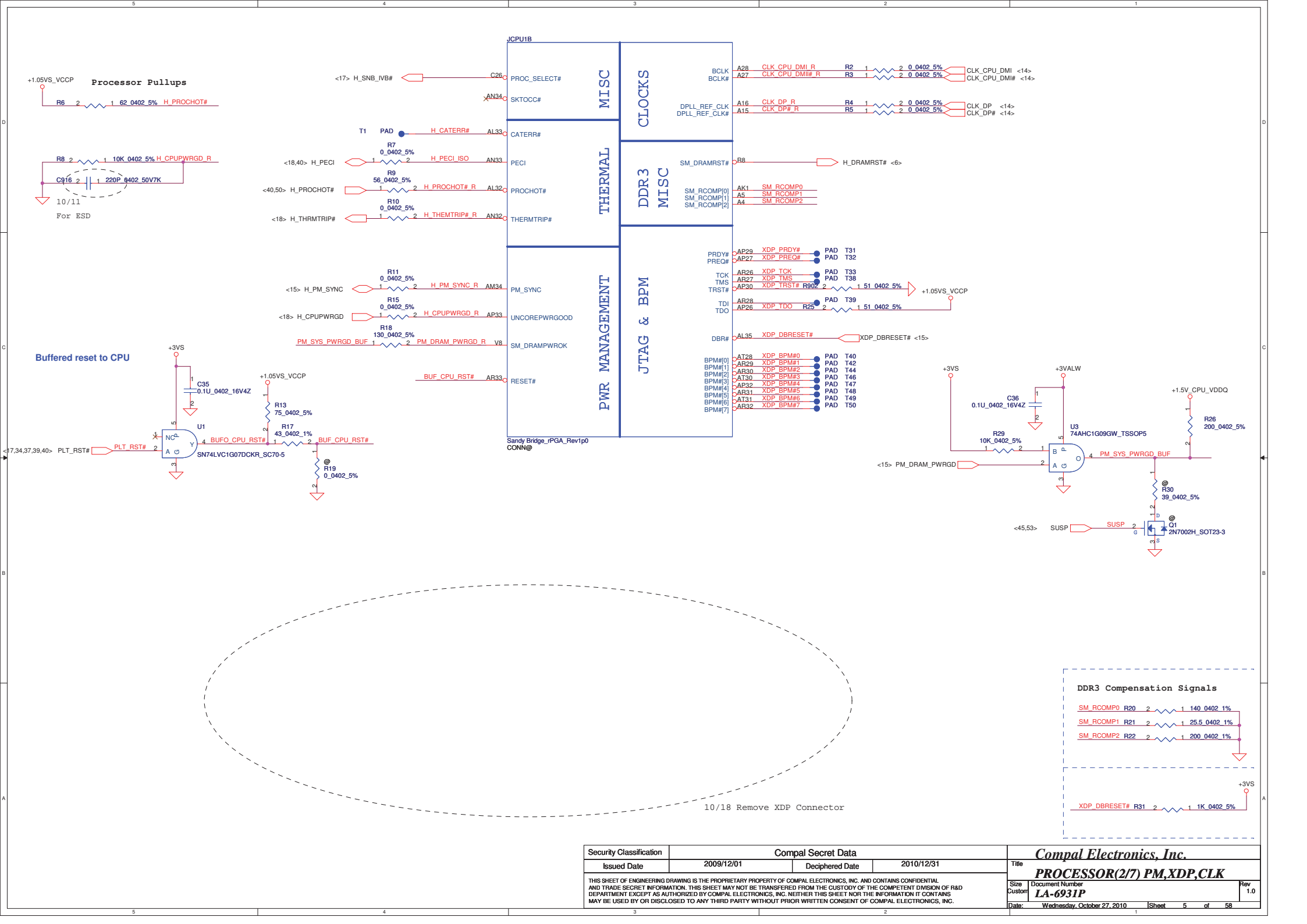
45@

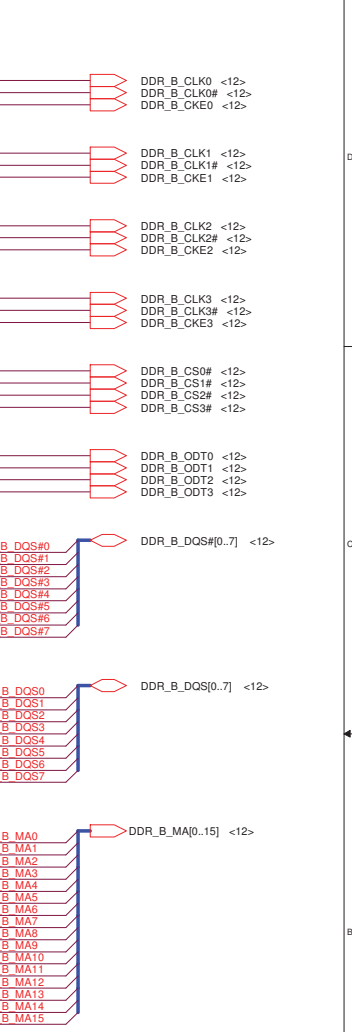
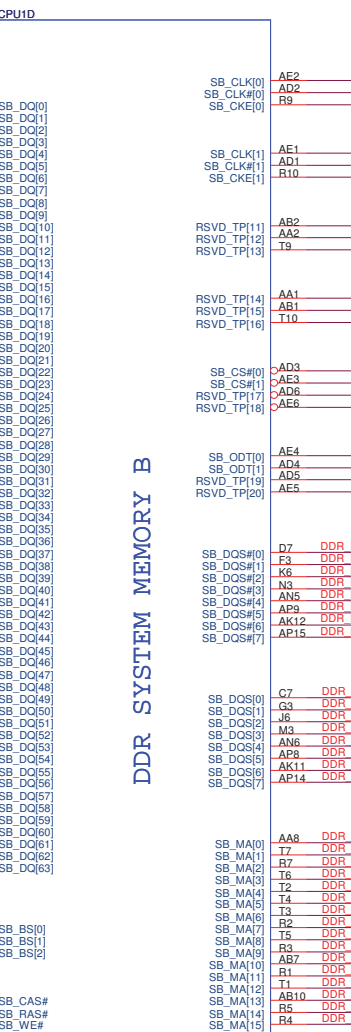
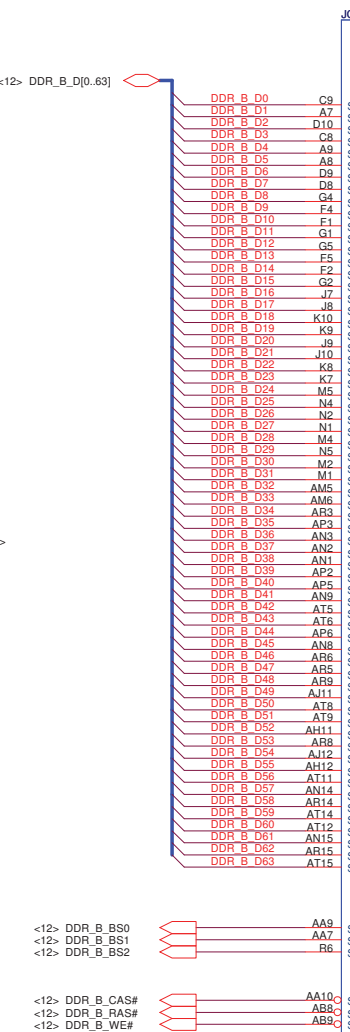
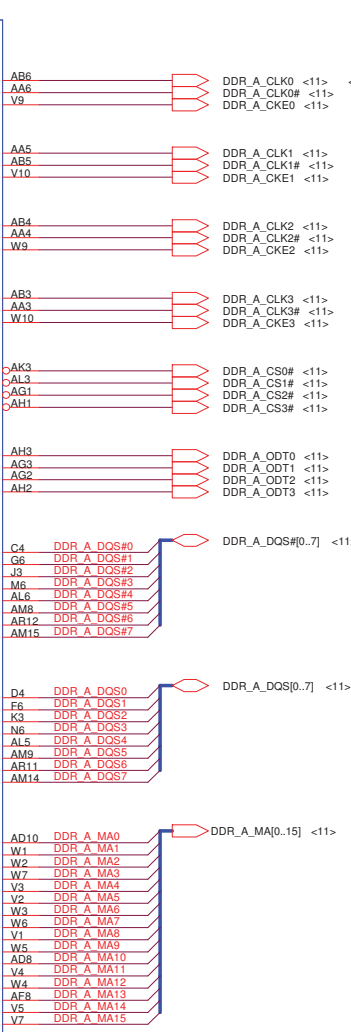
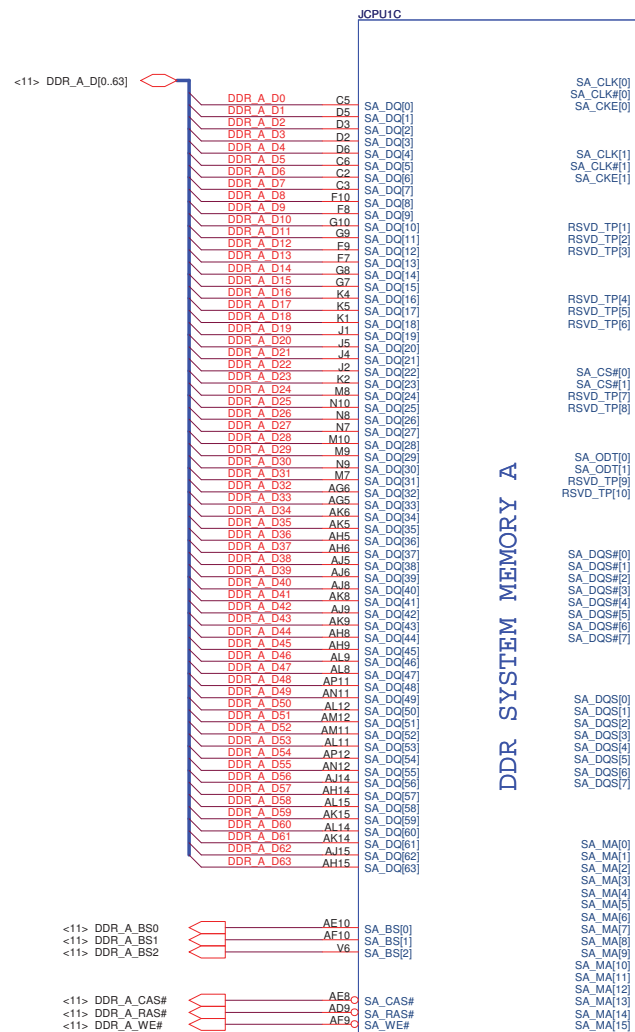
VRAM BOM Config

X76255BOL01: HYNIX 1G (old die)
X76255BOL02 HYNIX 1G (new die)
X76255BOL04 HYNIX 2G

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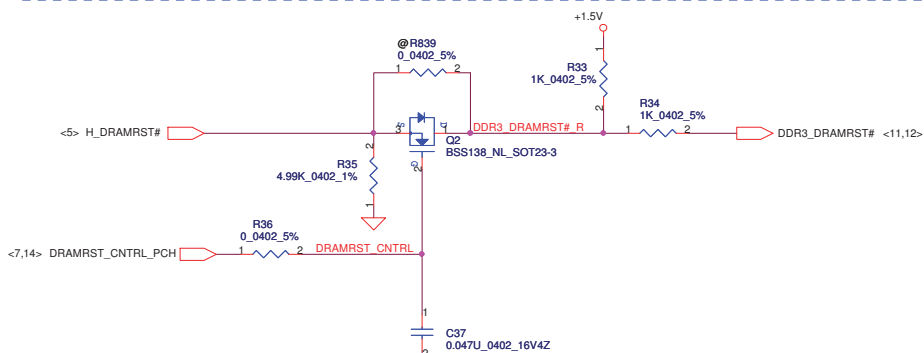


DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

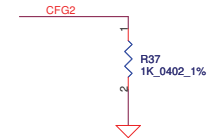
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CONN@

Sandy Bridge_rPGA_Rev1p0
CONN@

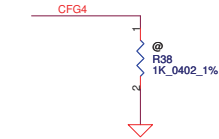


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2010/12/31				Title				PROCESSOR(3/7) DDRIII			
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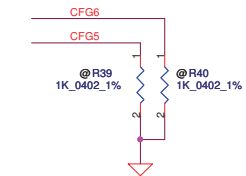
CFG Straps for Processor



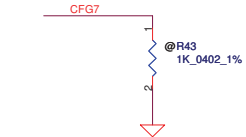
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



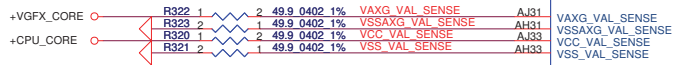
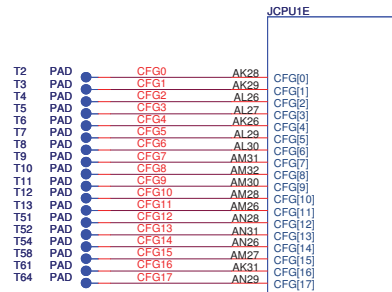
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



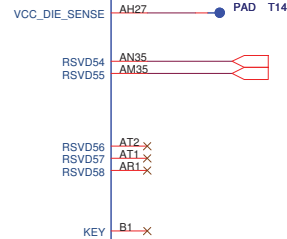
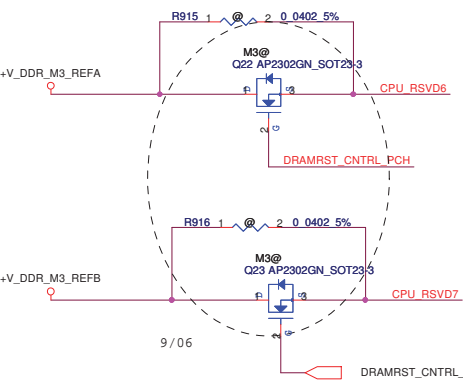
PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

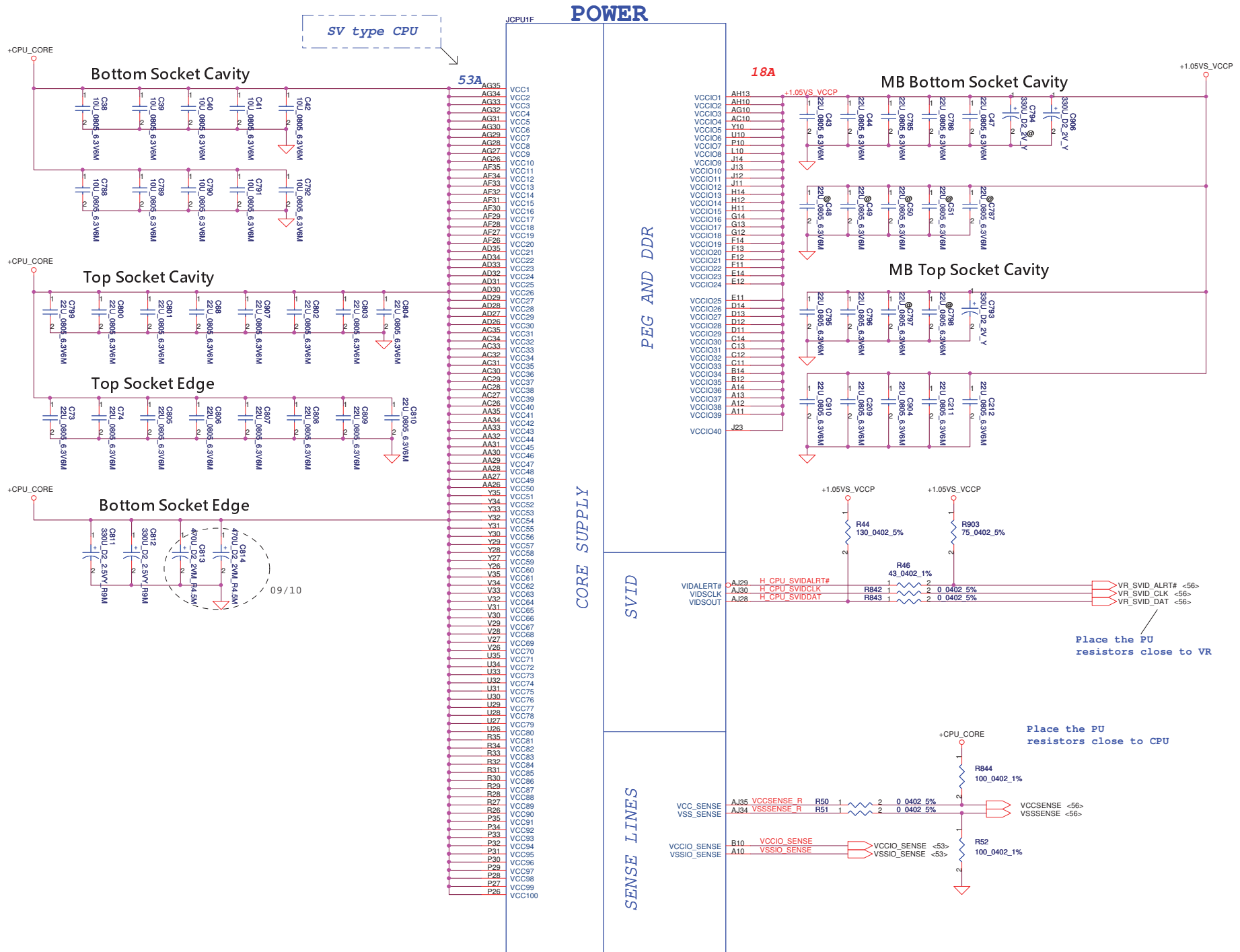


RESERVED

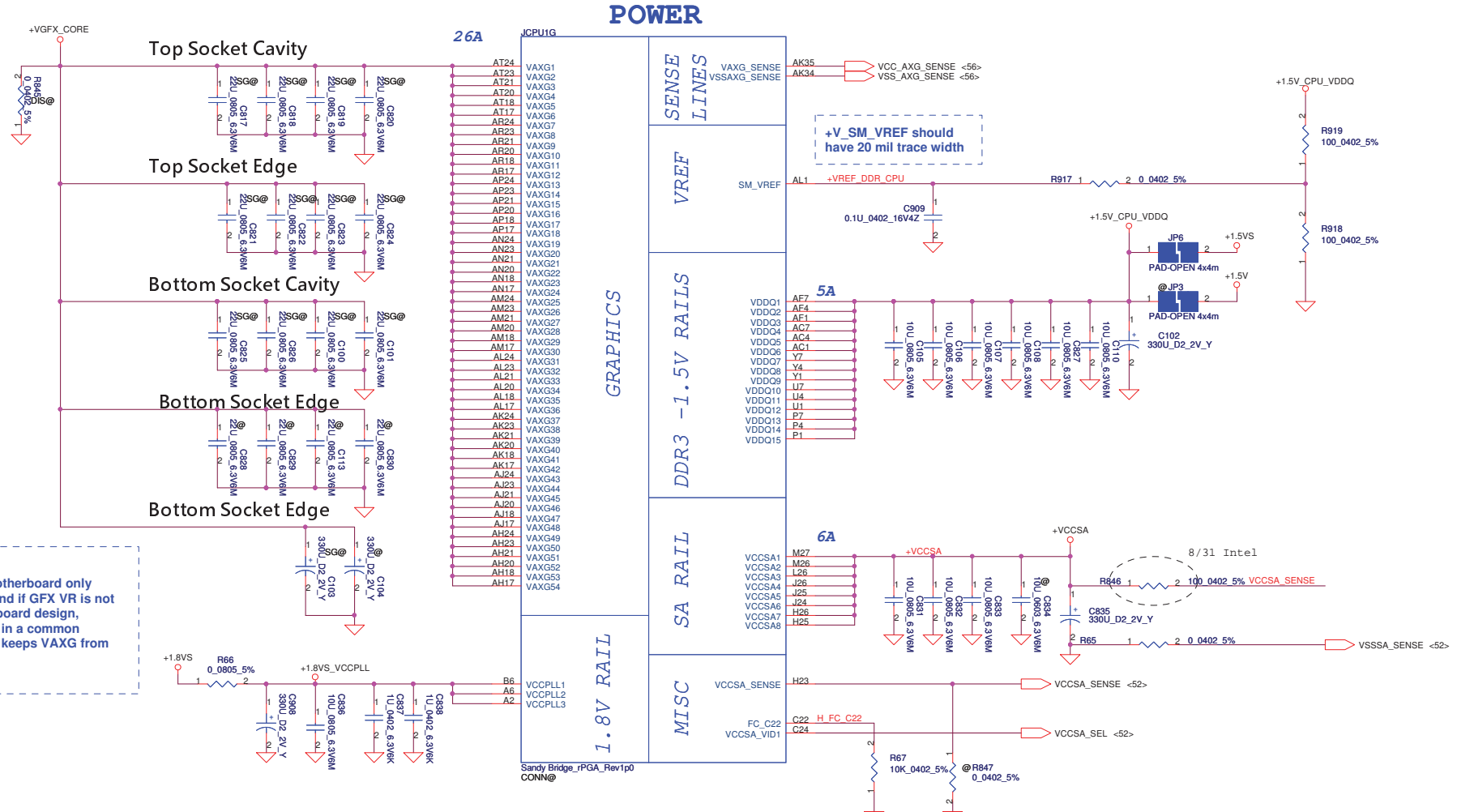
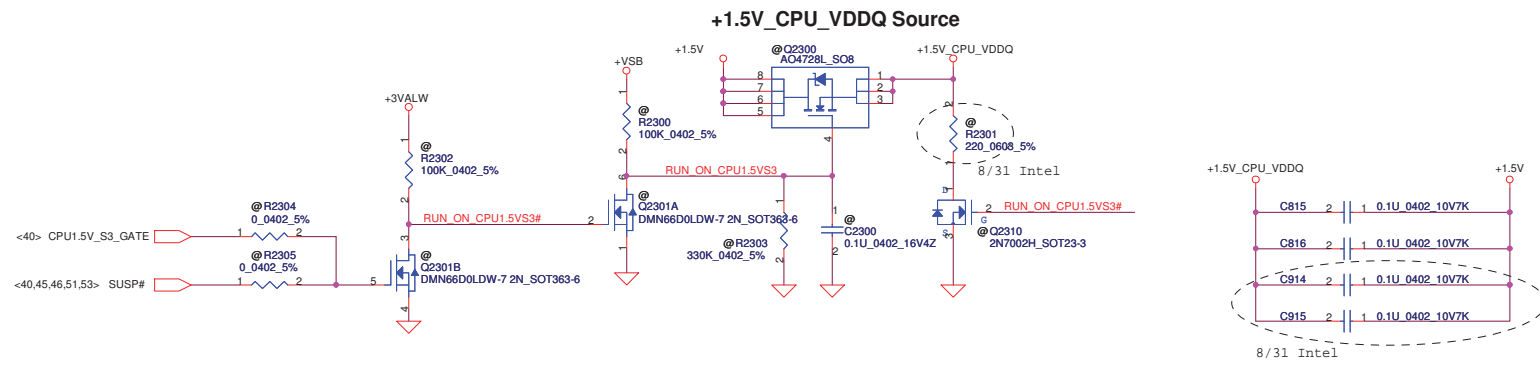


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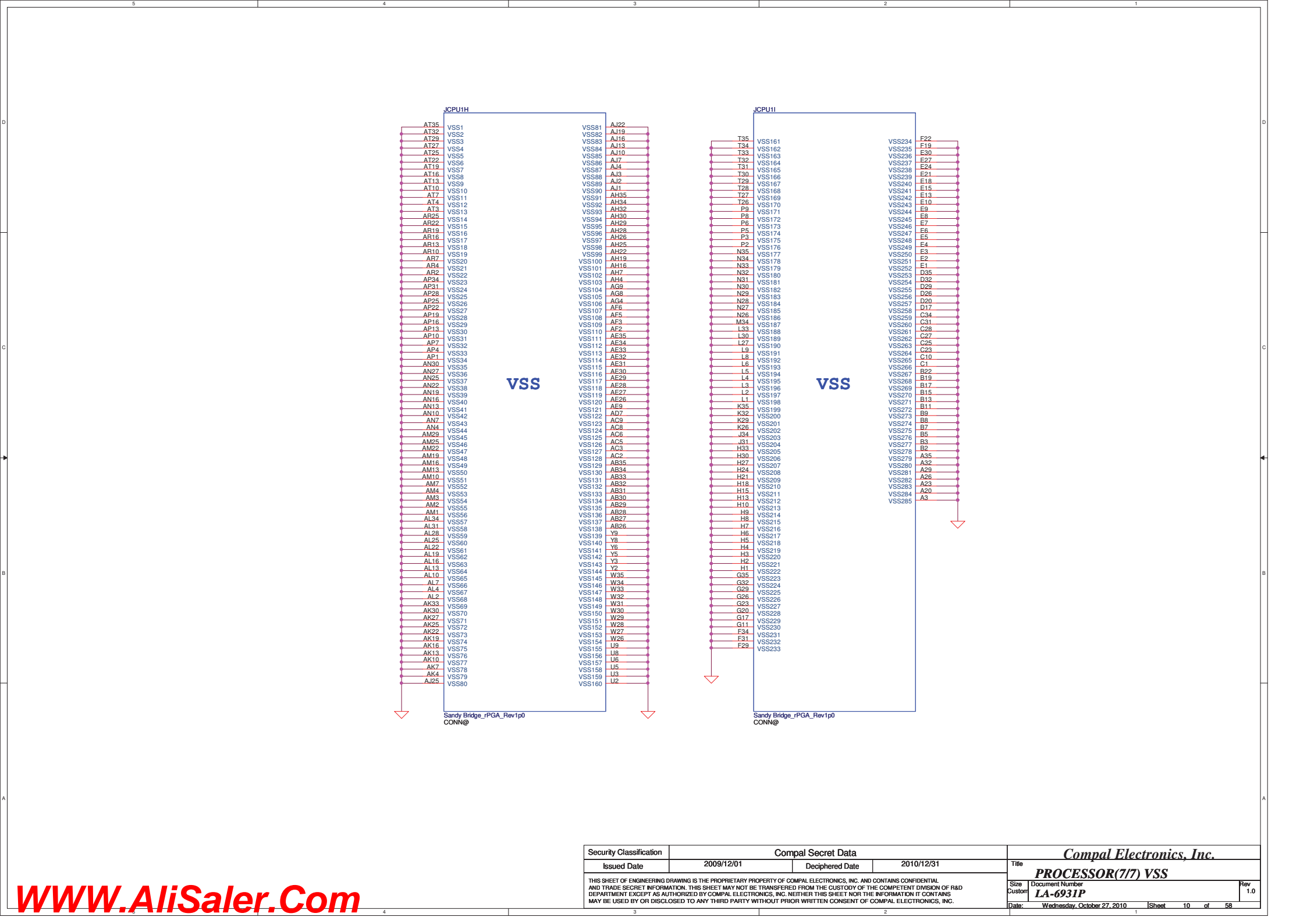
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CONN@

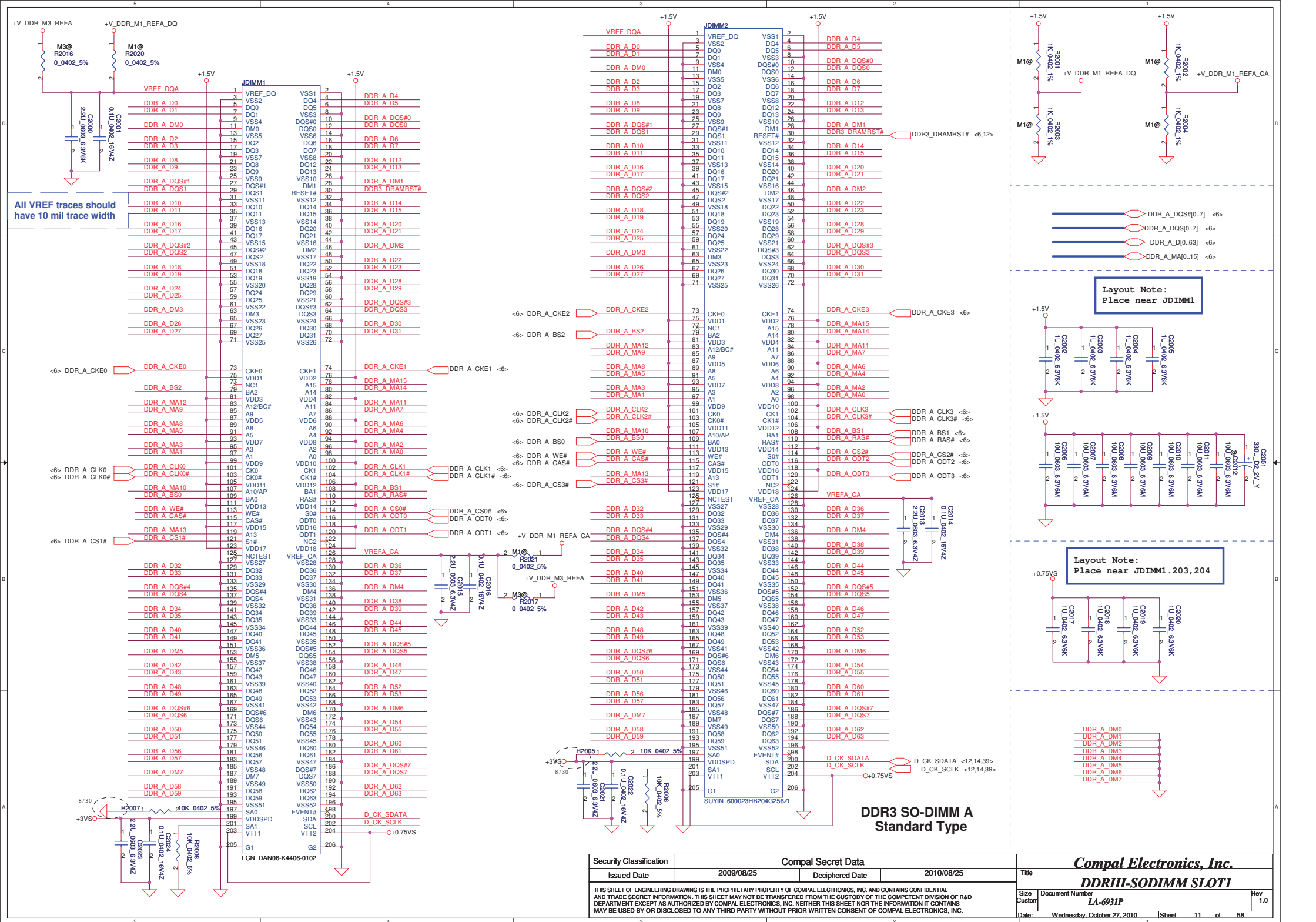


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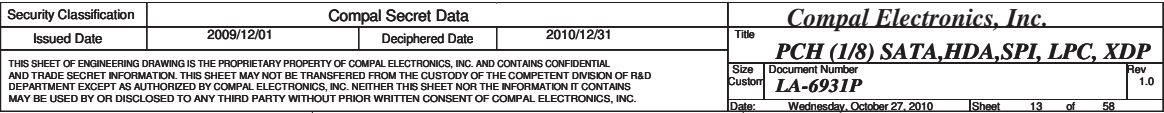


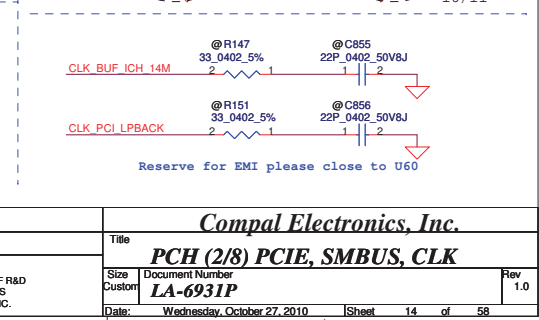
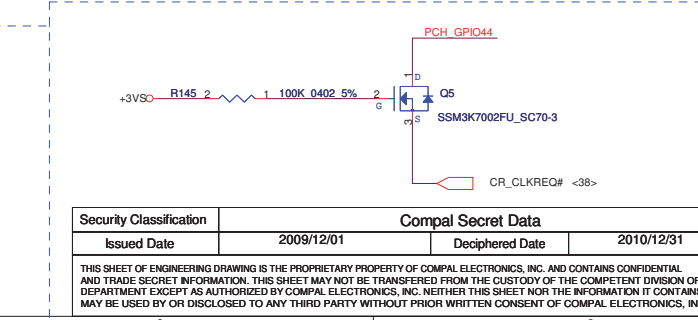
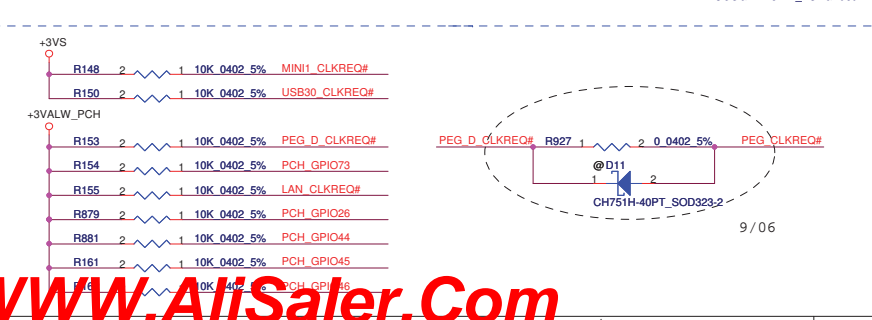
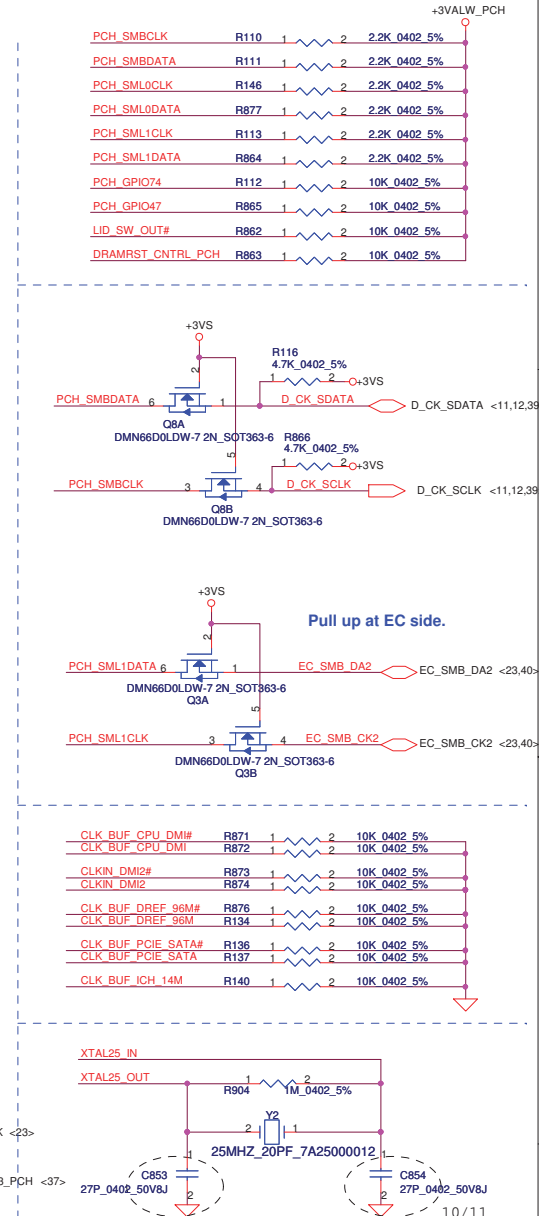
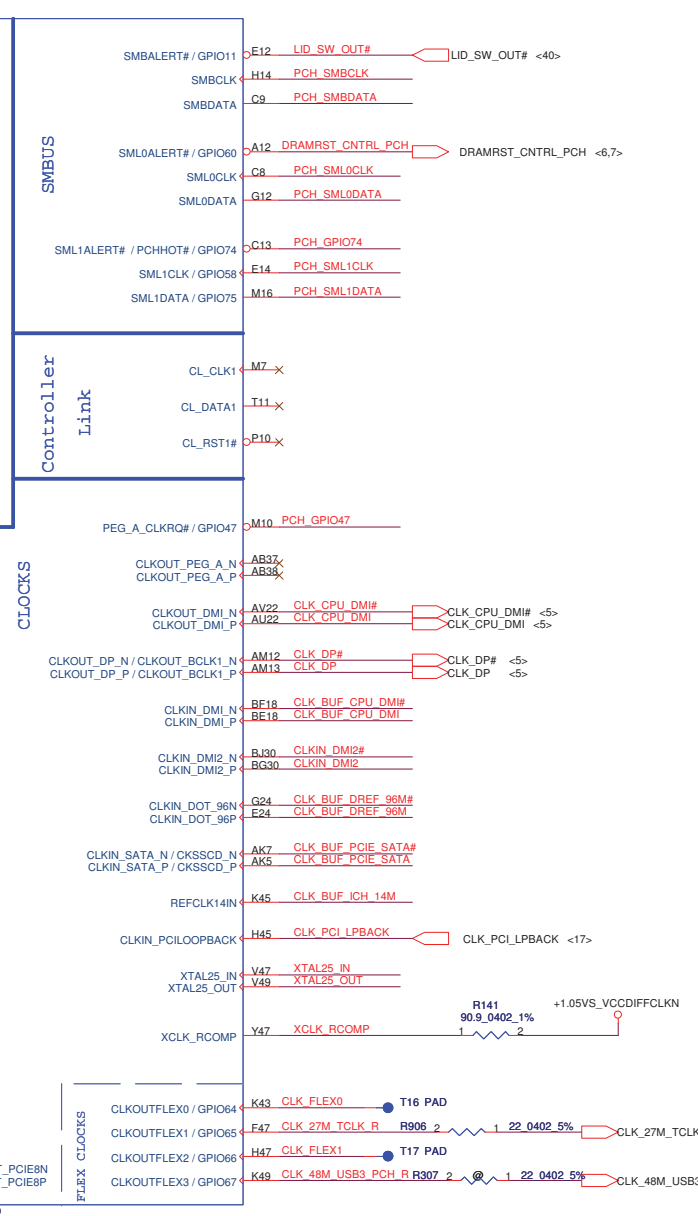
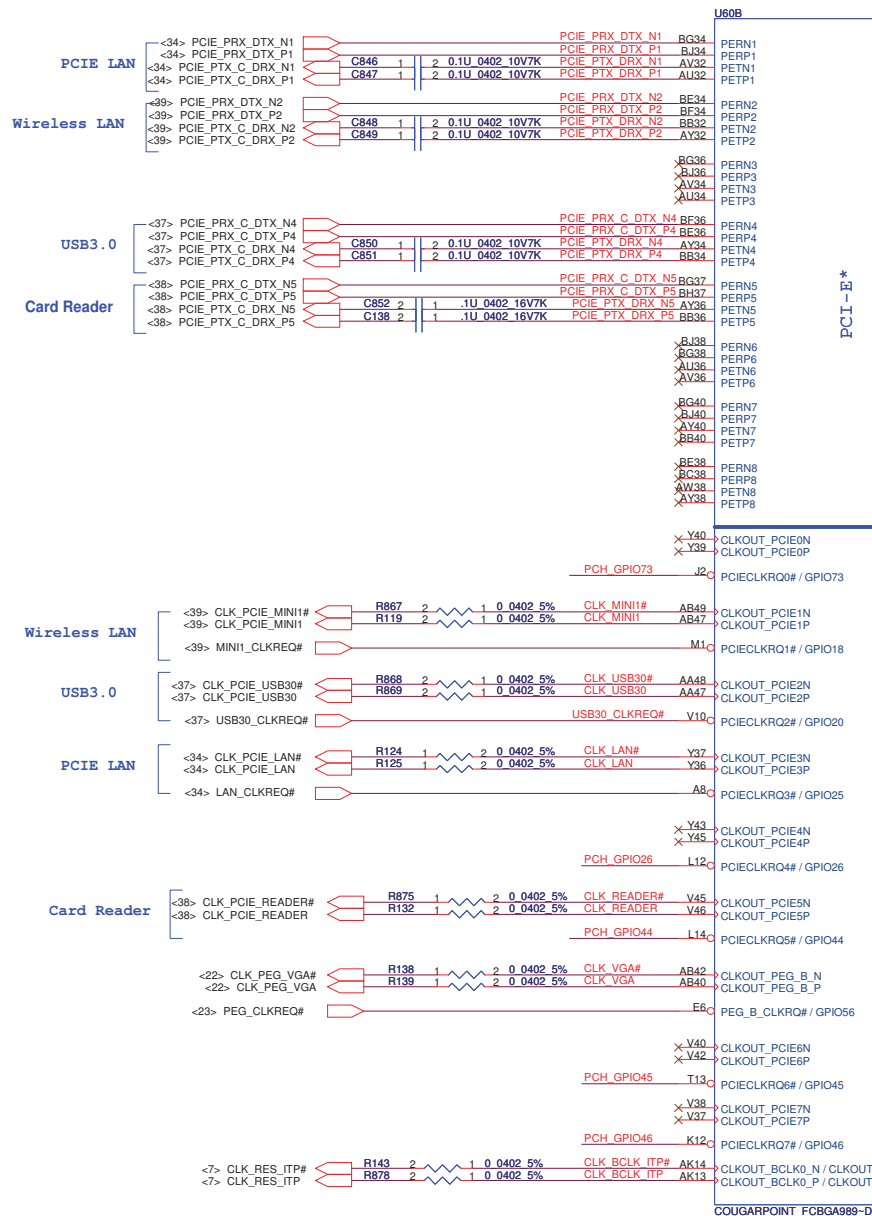
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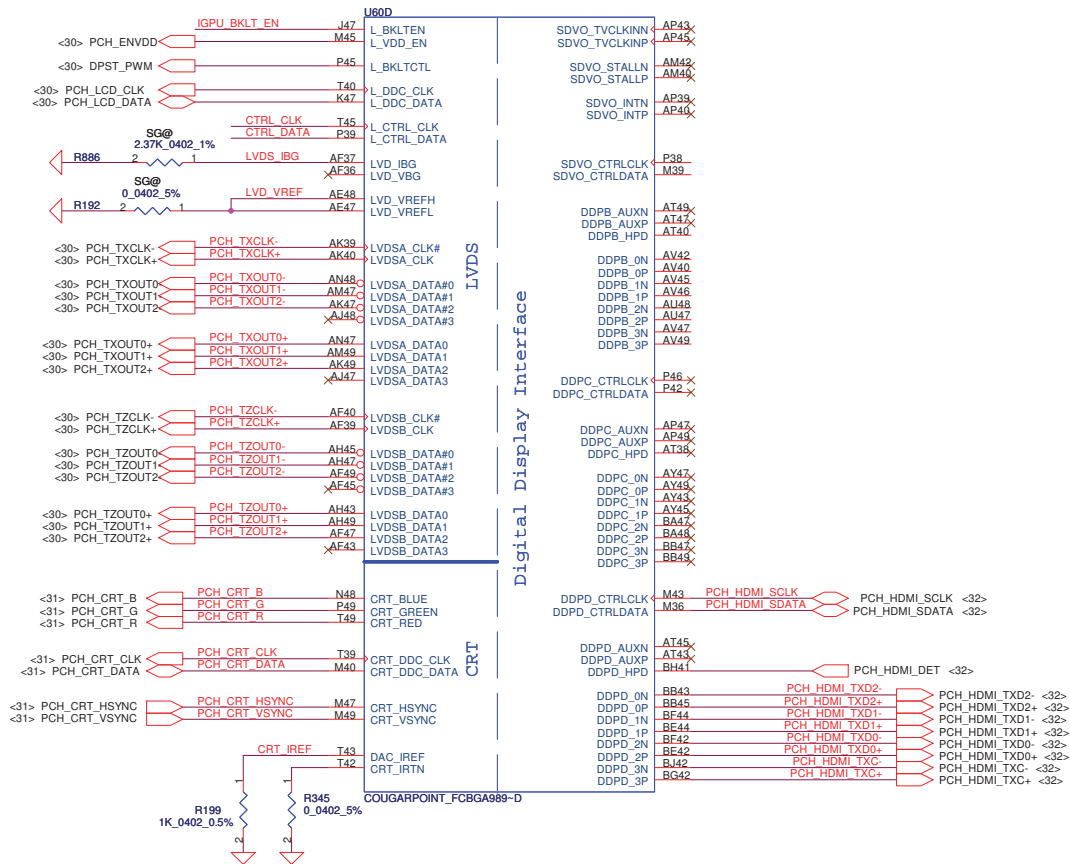
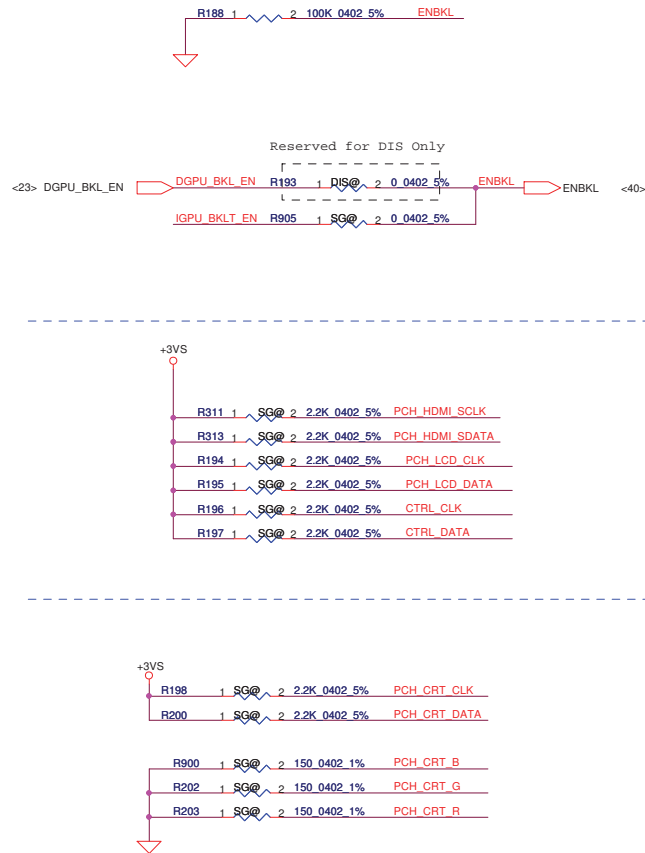




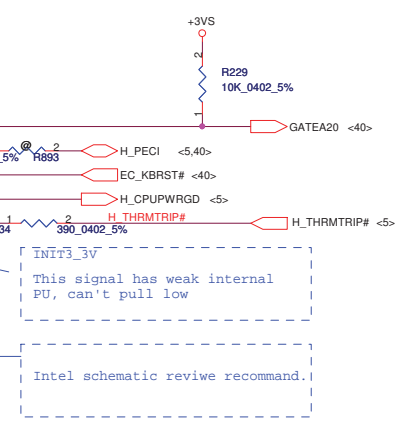
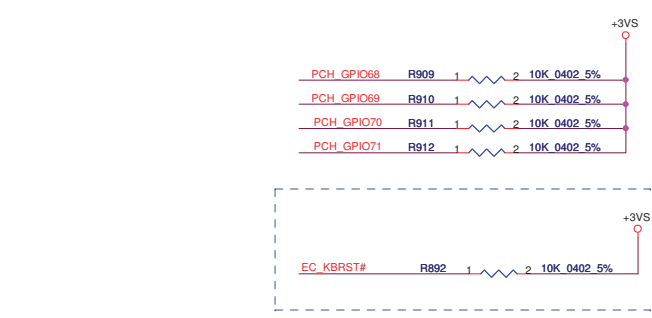
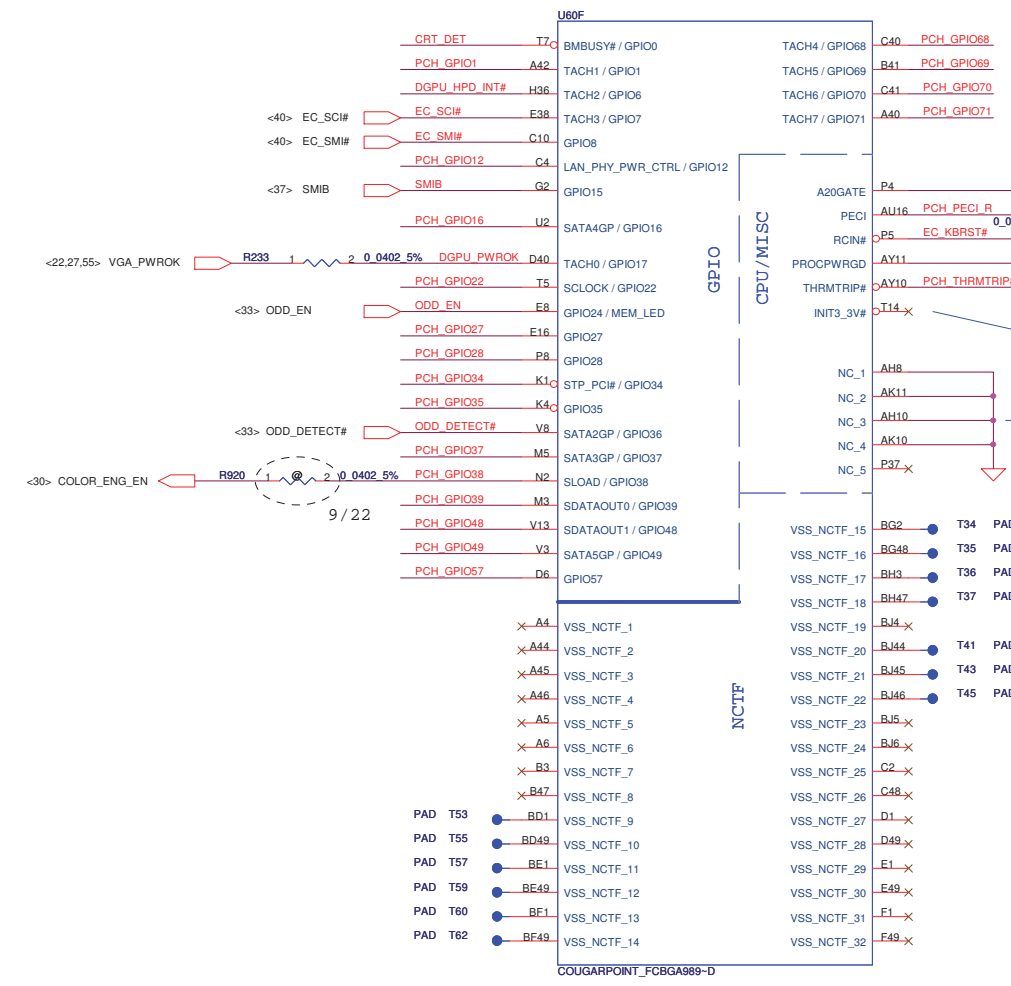
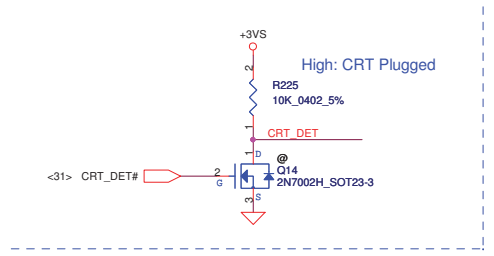
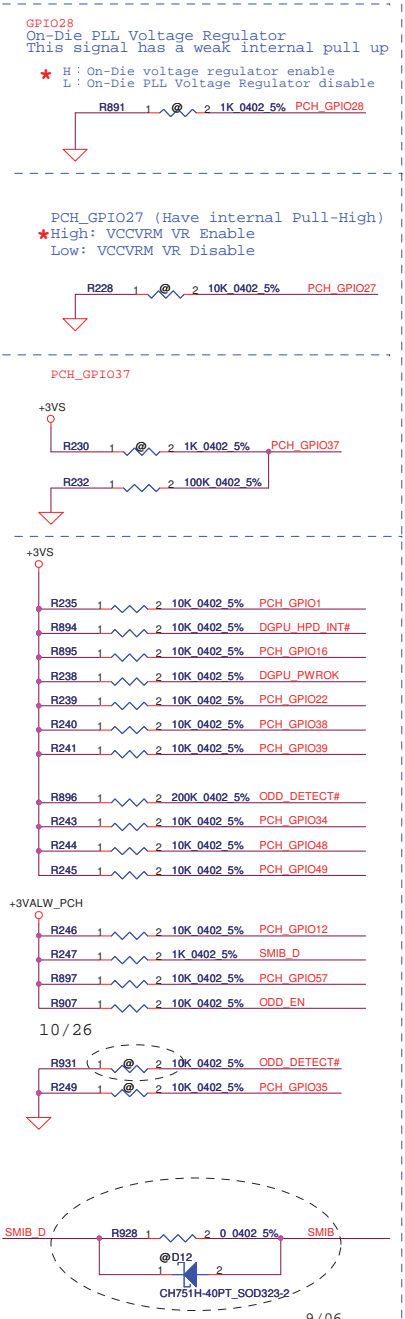




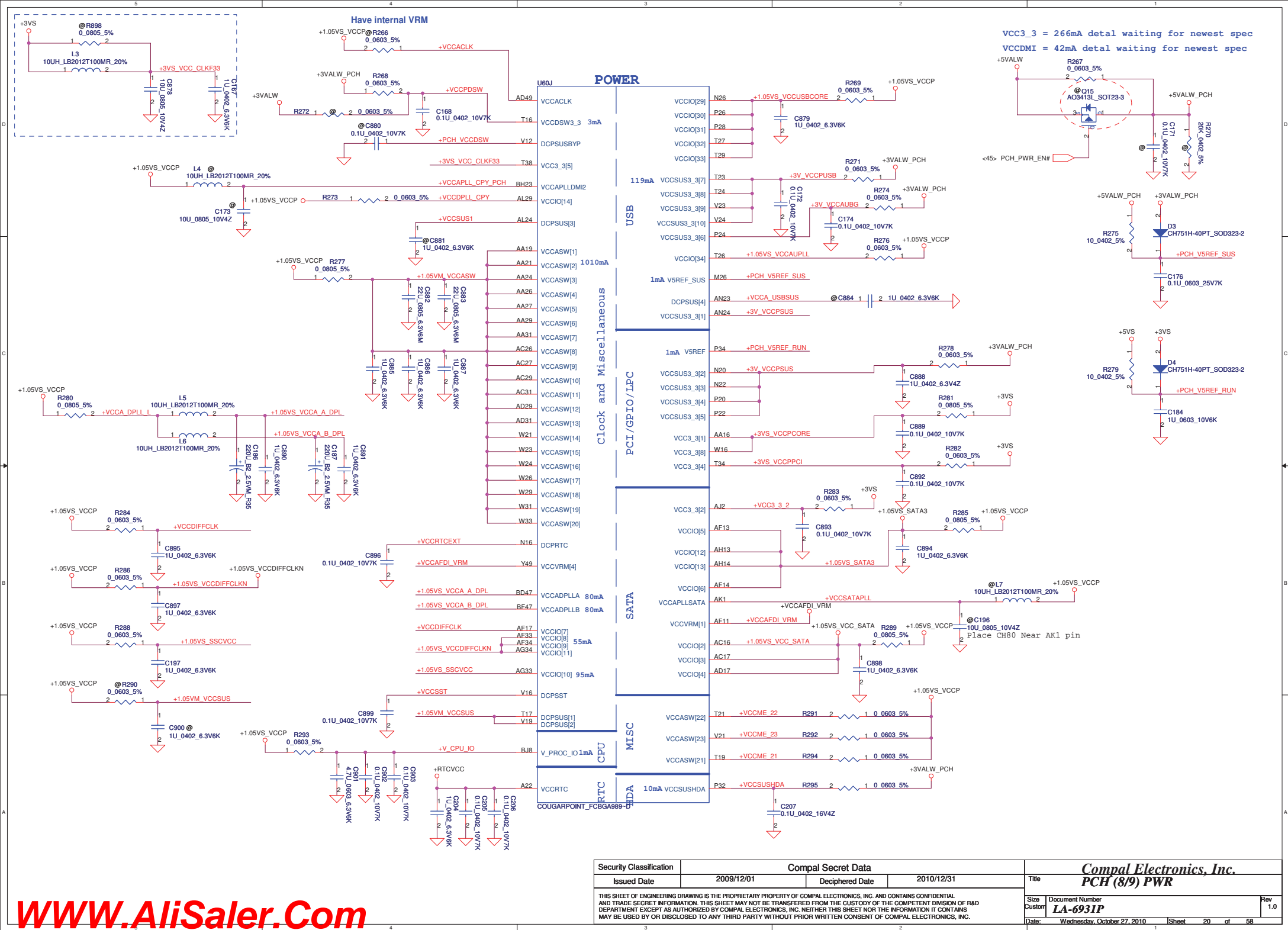
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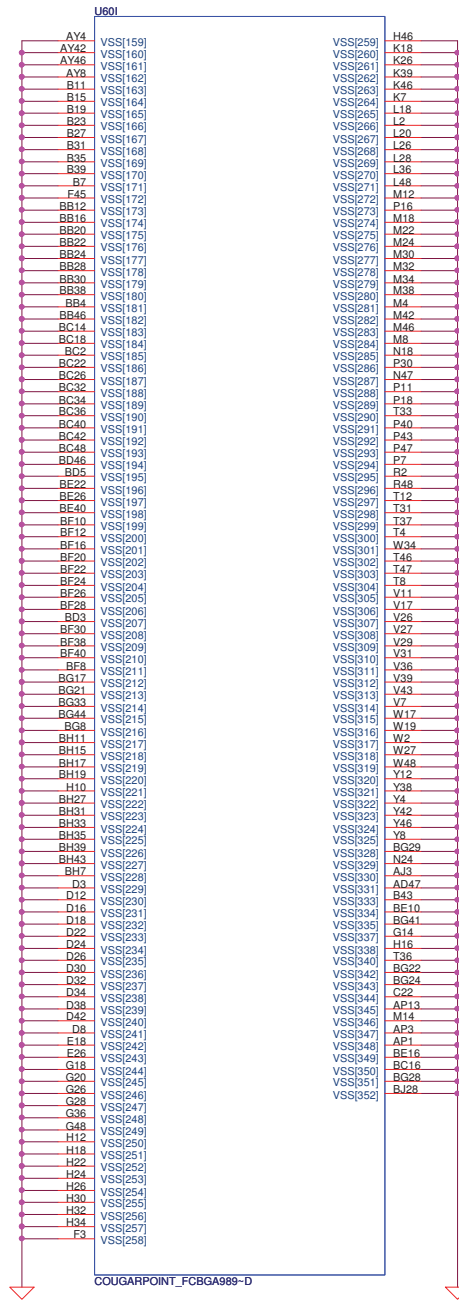
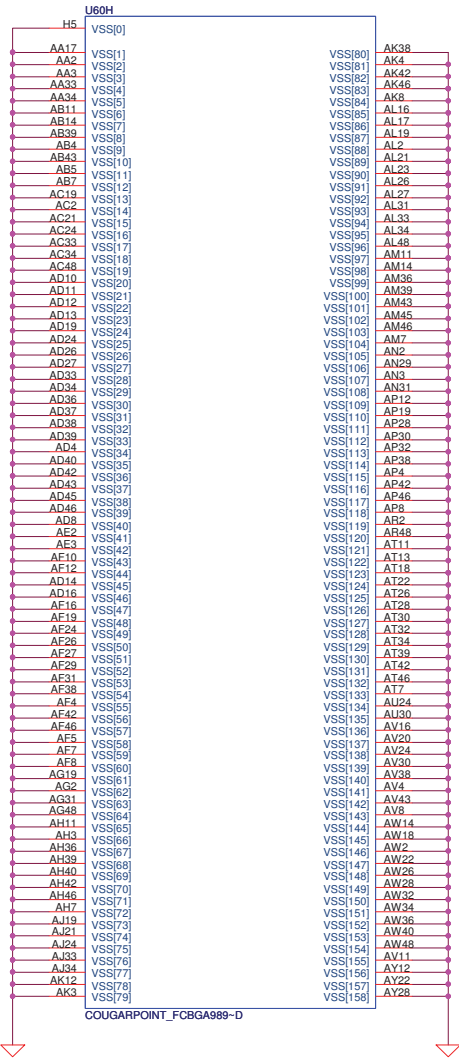


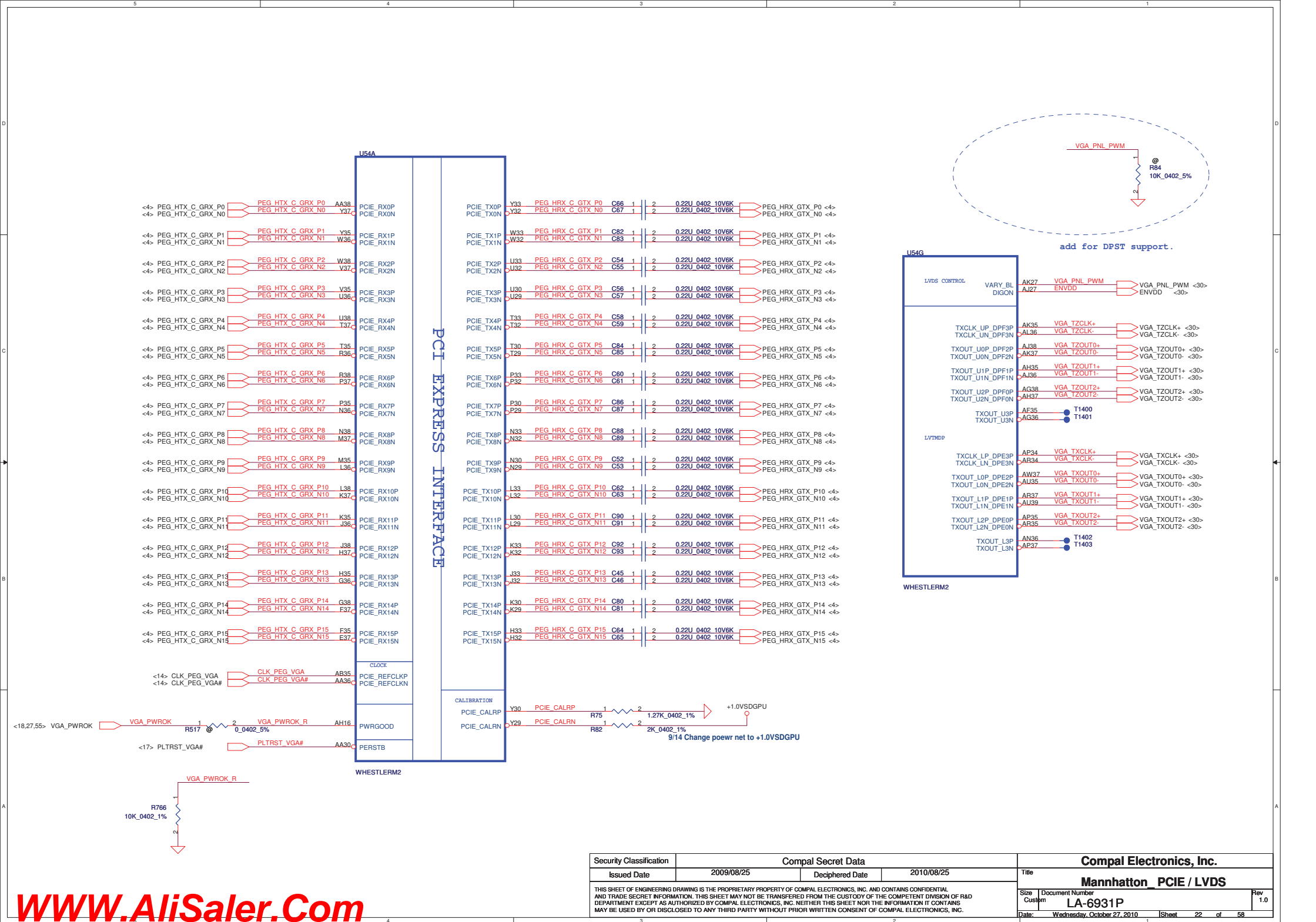
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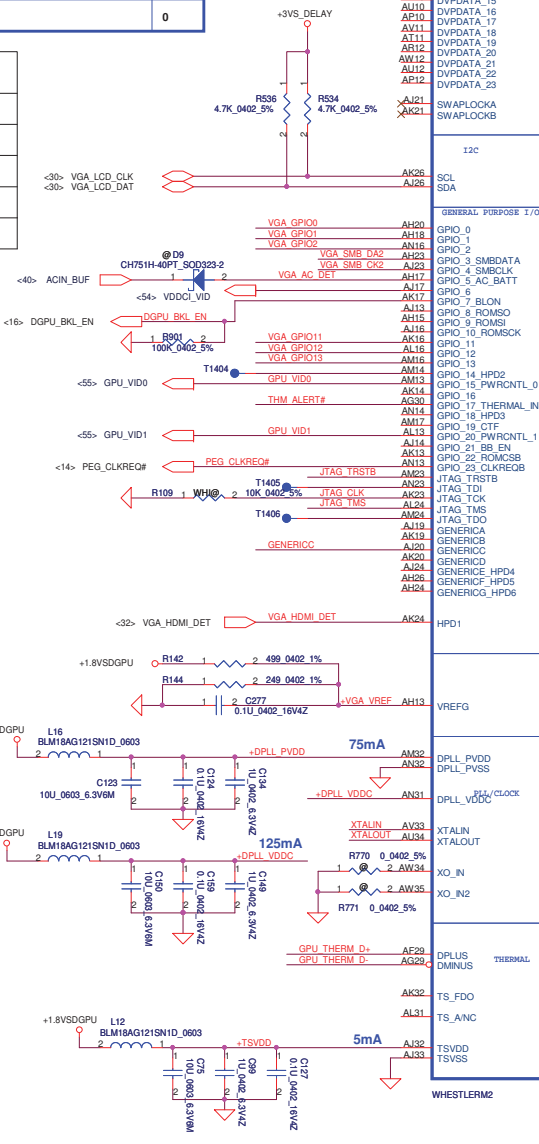
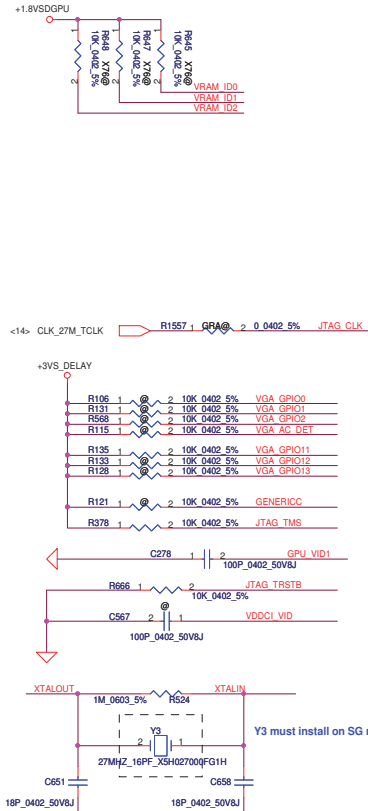






Strap Name		Pin Straps description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
CONFIG[1] CONFIG[2] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
SMS_EN_HARD	H2SYNC	Can be unconnected if not used.	0
VIP_DEVICE _STRAP_DIS	V2SYNC	Can be unconnected if not used.	0

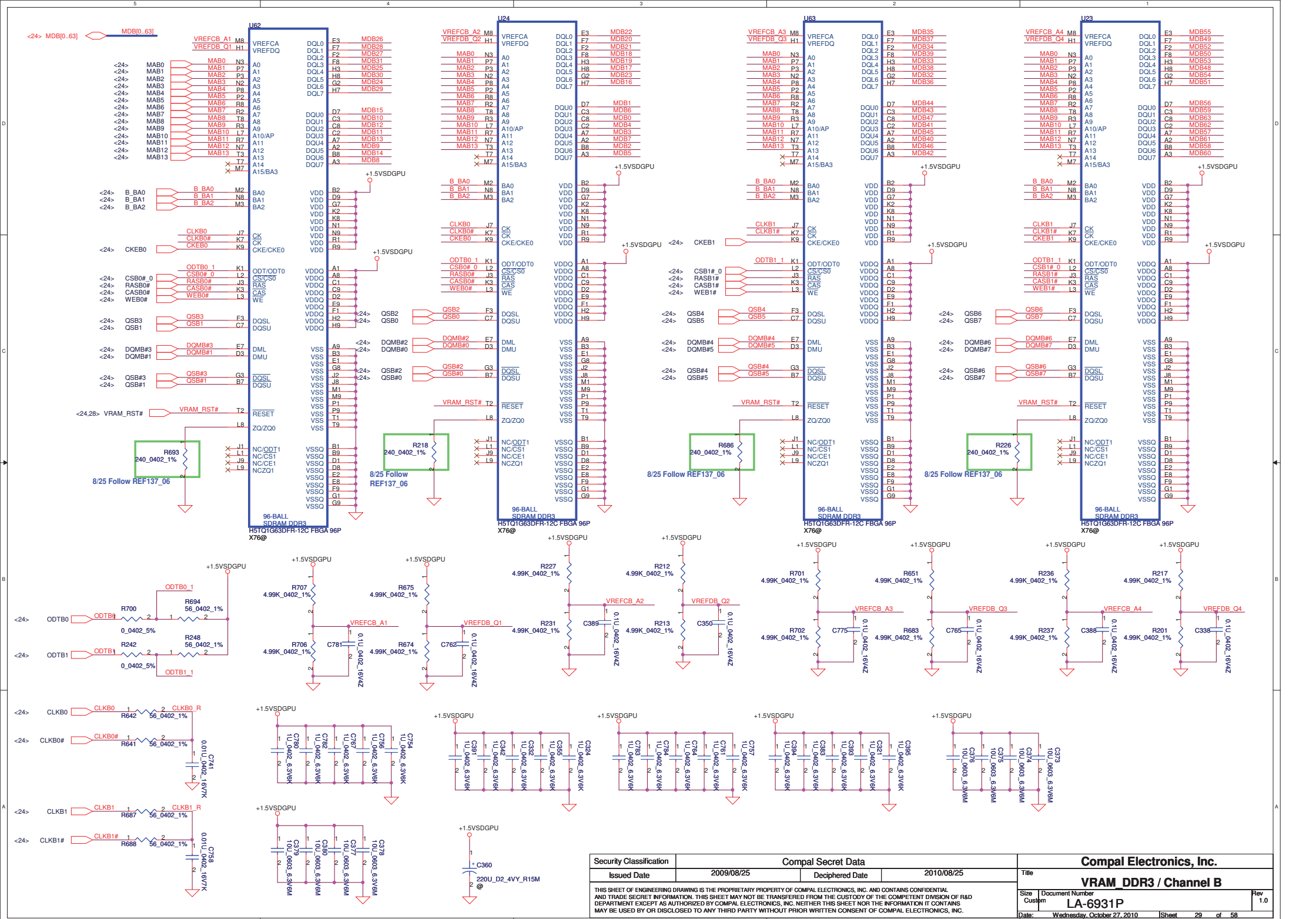
VRAM	Location	VRAM_ID2	VRAM_ID1	VRAM_ID0
Hynix(8pcs) 1GB (old) H5TQ1G63BFR-12C		0	0	1
Hynix(8pcs) 1GB (900MHz) H5TQ1G63DFR-11C		0	1	0
Samsung(8pcs) 1GB (800MHz) K4W1G1646G-BC11 LF		0	1	1
Hynix(8pcs) 2GB (800MHz) H5TQ2G63BFR-12C		1	0	0
Samsung(8pcs) 2GB (800MHz) K4W2G1646C-HC12		1	0	1



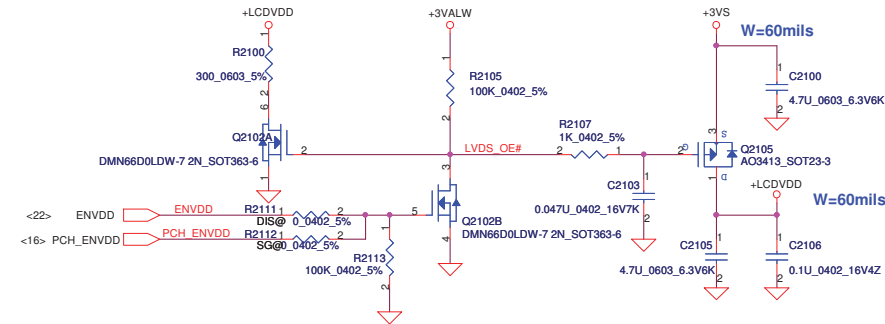


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				Size	Document Number	Rev
				Custom	LA-6931P	1.0
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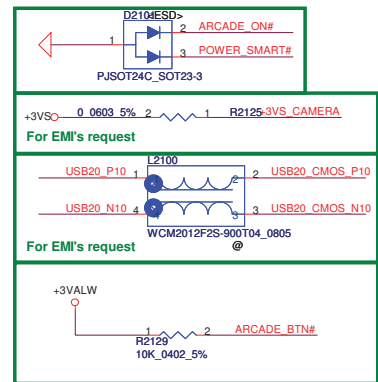
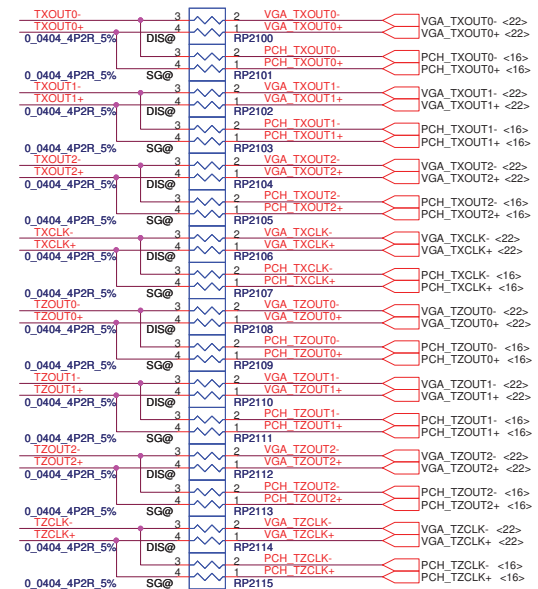
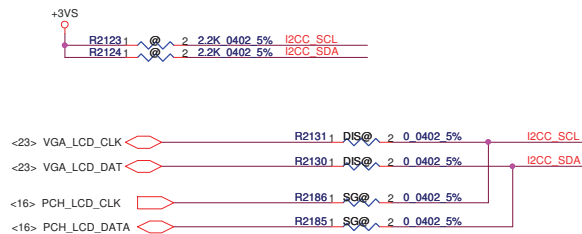
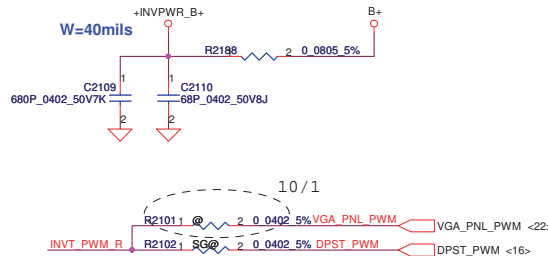
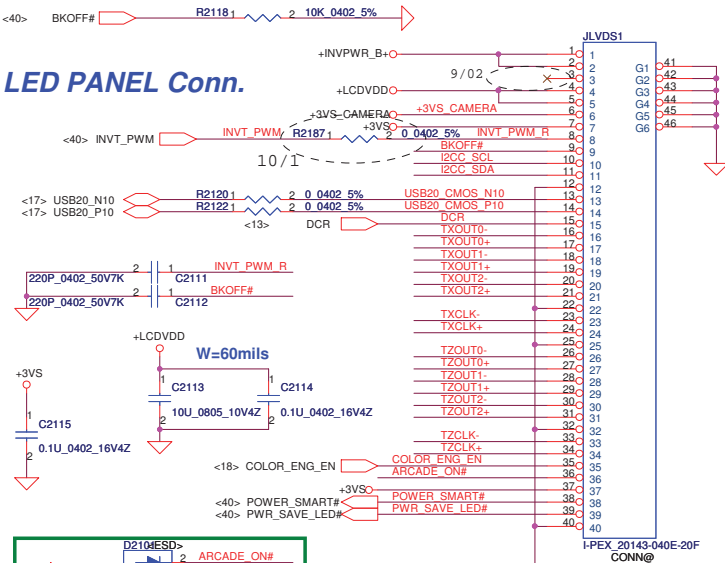




LCD POWER CIRCUIT



LED PANEL Conn.

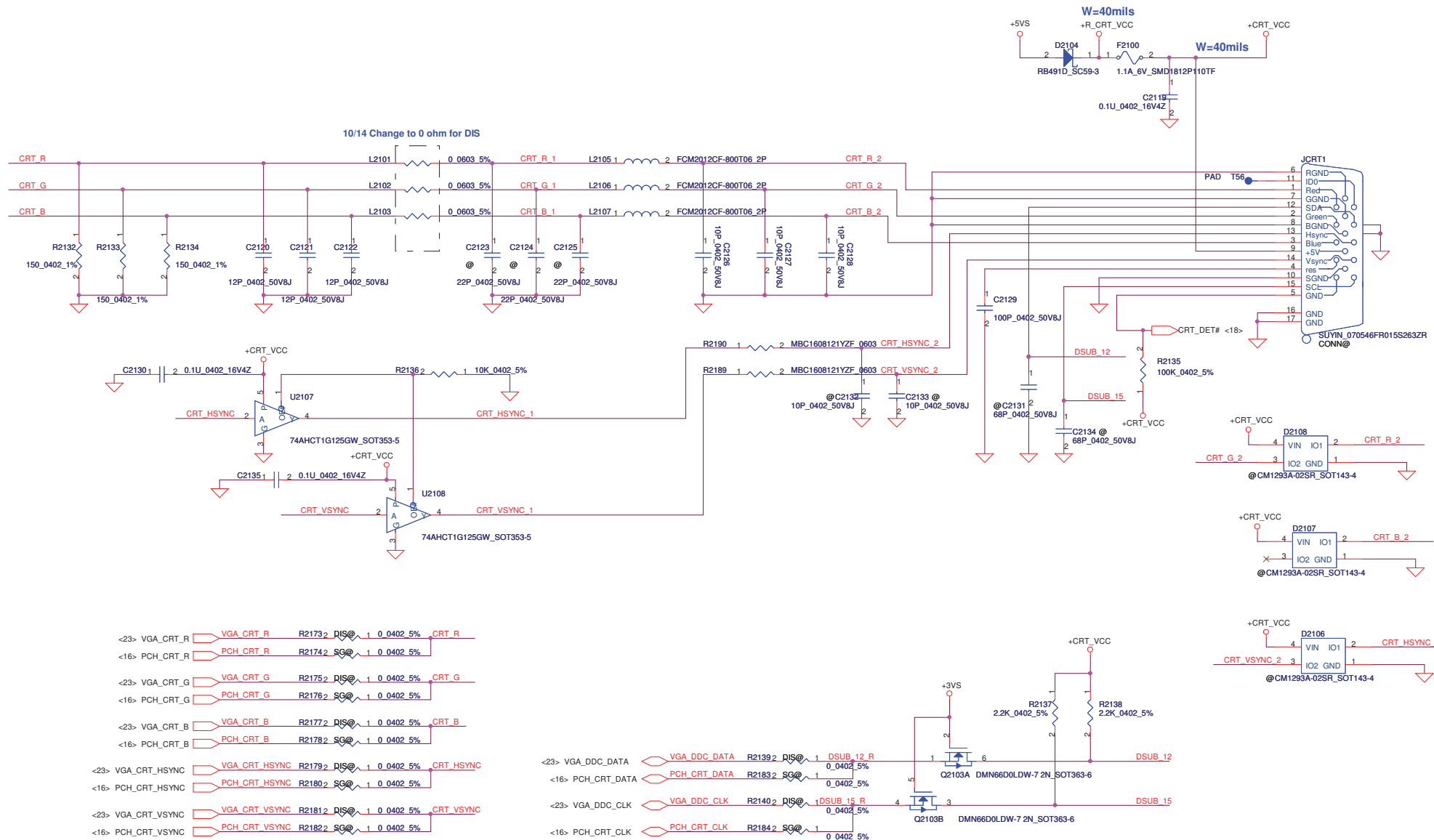


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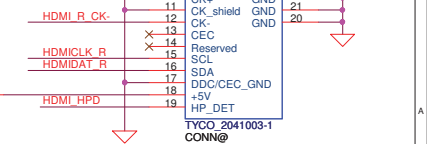
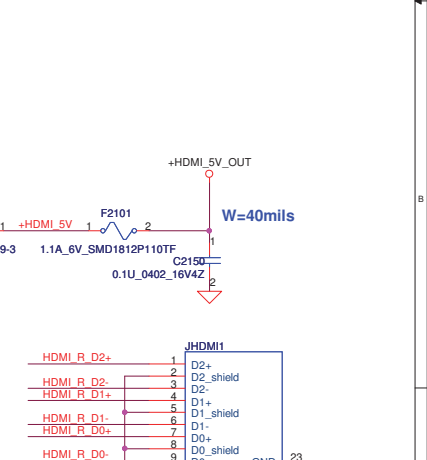
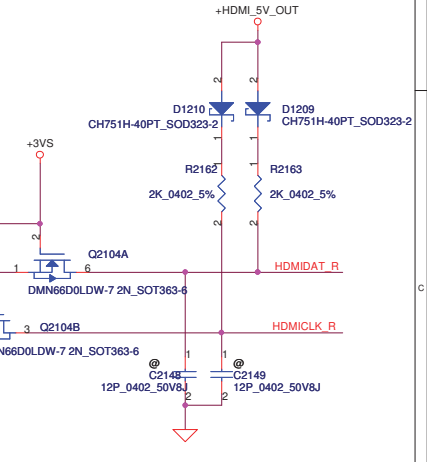
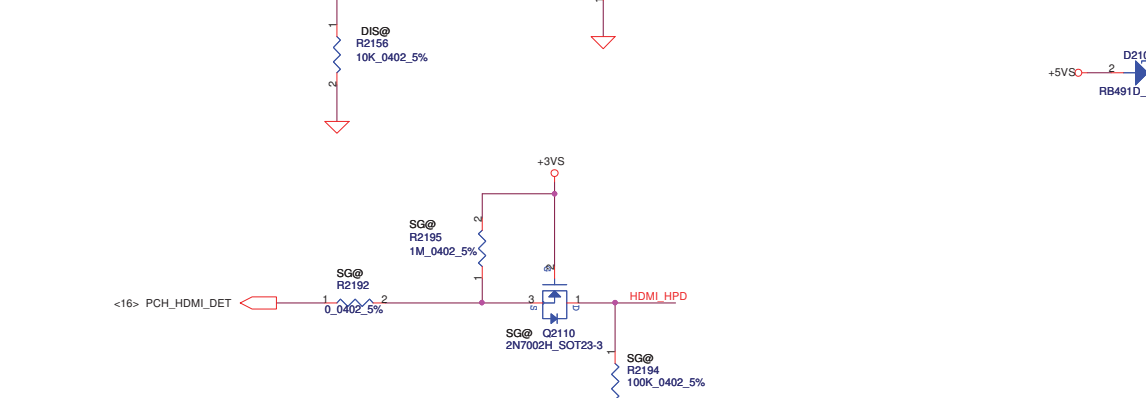
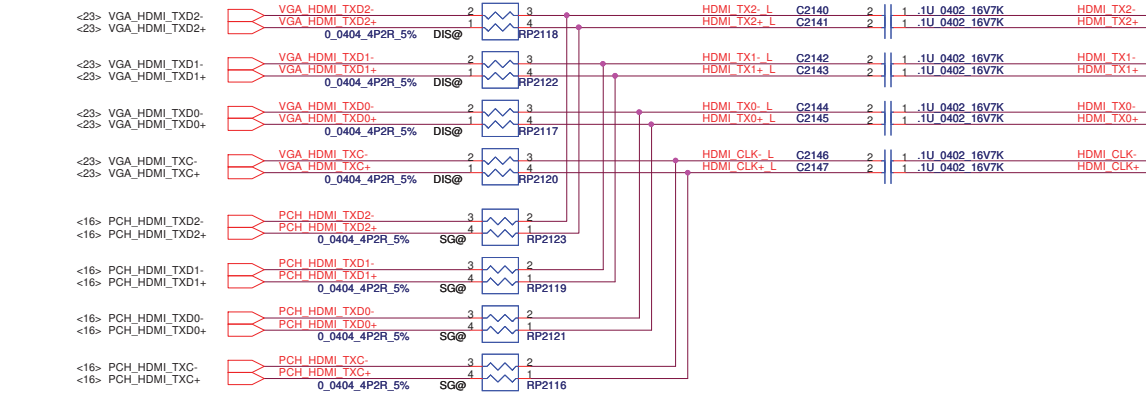
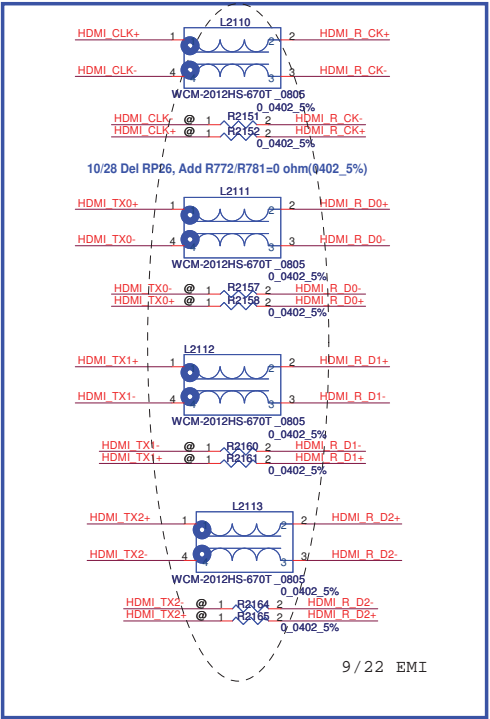
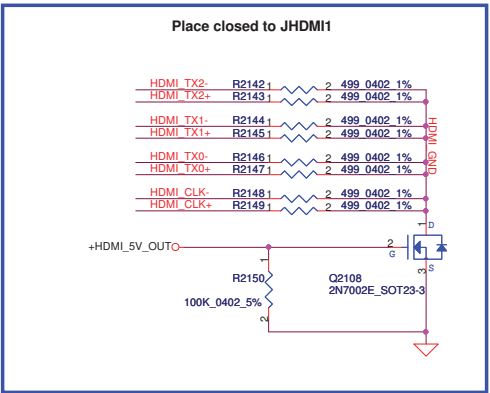
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Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title	
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				Size	Document Number
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				Rev	1.0

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CRT Connector



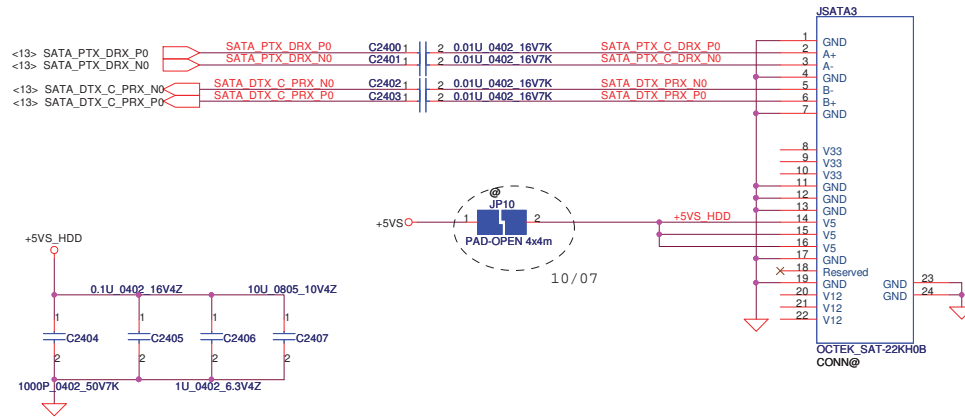
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2009/08/25	Deciphered Date	2009/08/25	Title	CRT Connector		
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Issued Date				2009/08/25				HDMI Level Shife & Conn			
Deciphered Date				2010/08/25				LA-6931P			
Title				Size				Rev			
Date				Wednesday, October 27, 2010				1.0			
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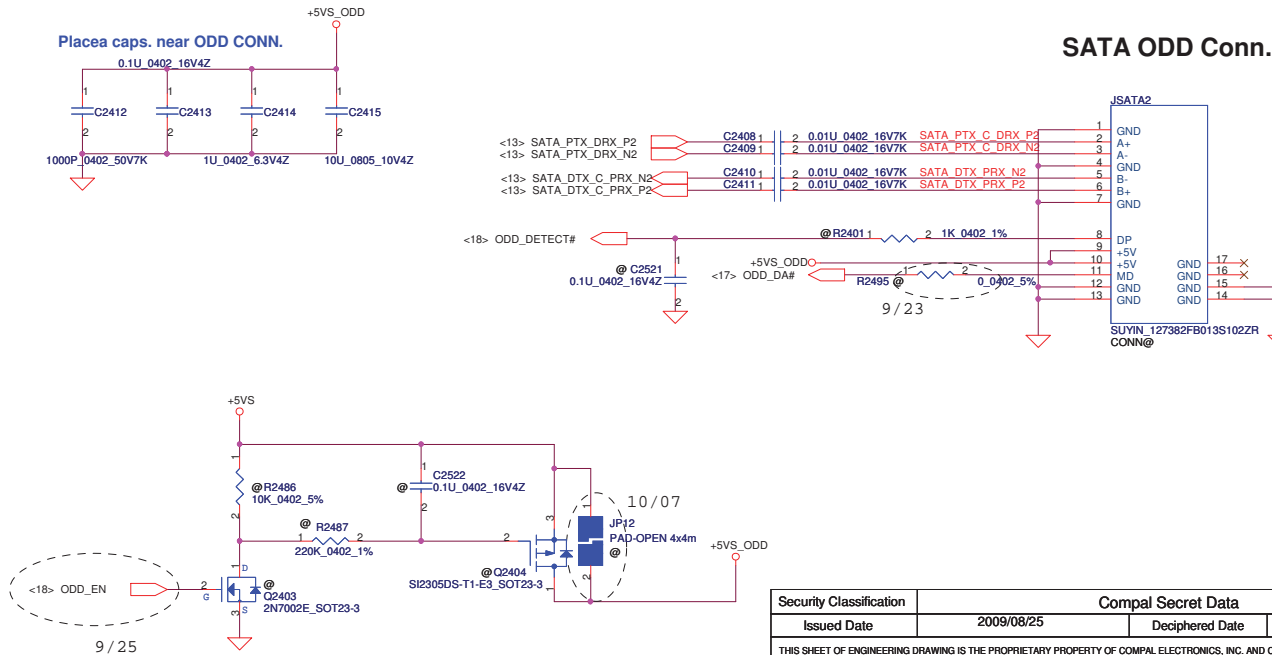
HDD

SATA HDD Conn.

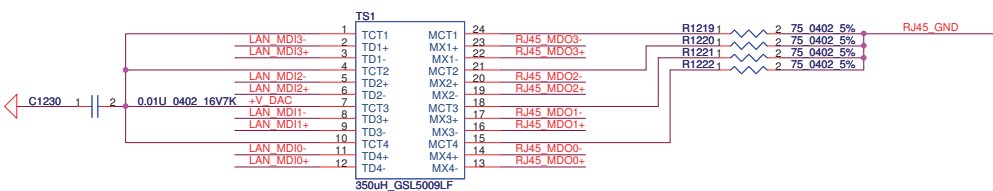
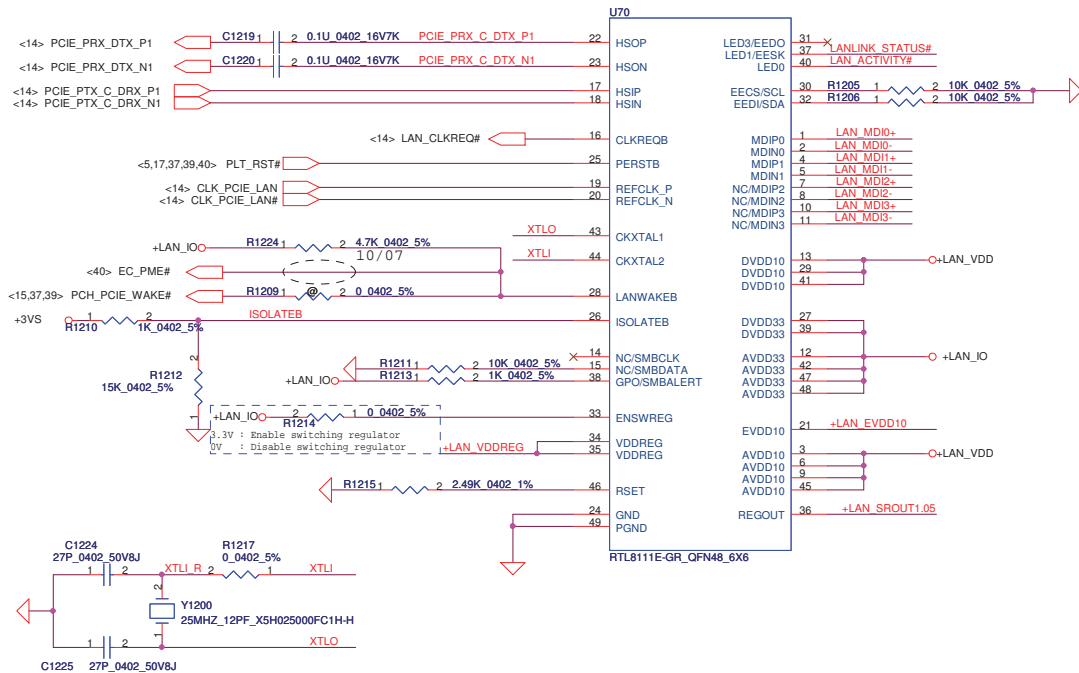
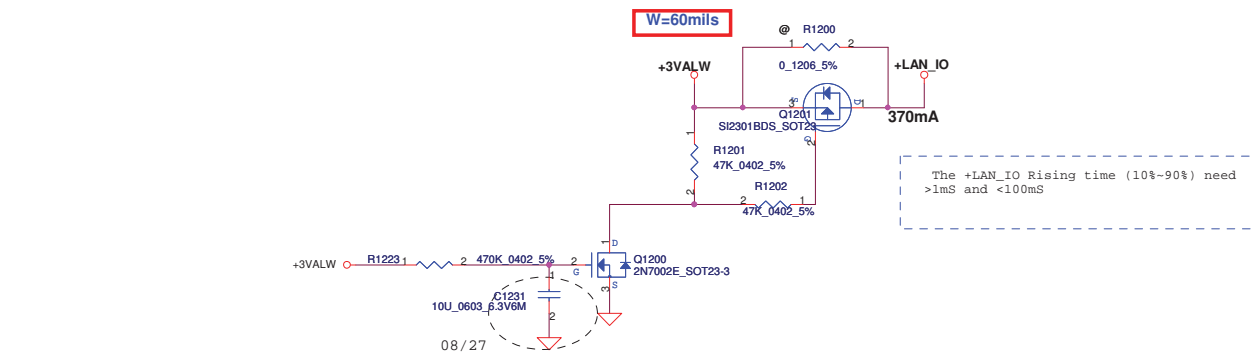


ODD

SATA ODD Conn.

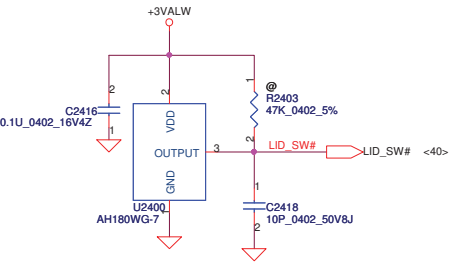


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								2010/08/25			
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								HDD & ODD Connector			
Size B				Document Number				Rev 1.0			
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Date:				Wednesday, October 27, 2010				Sheet 33 of 58			

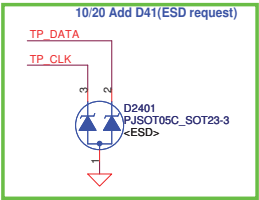
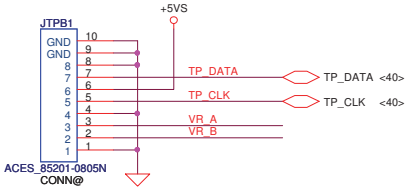
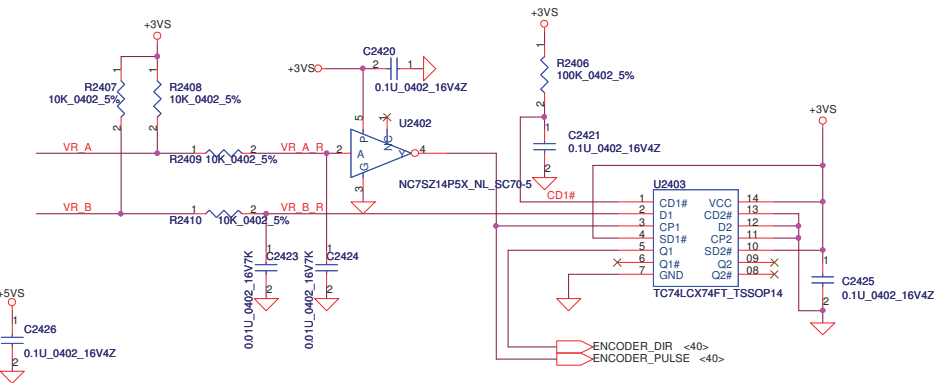


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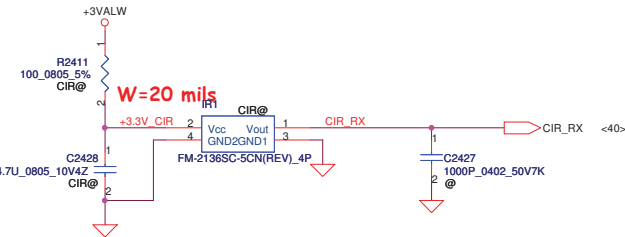
Lid Switch



Touch Pad

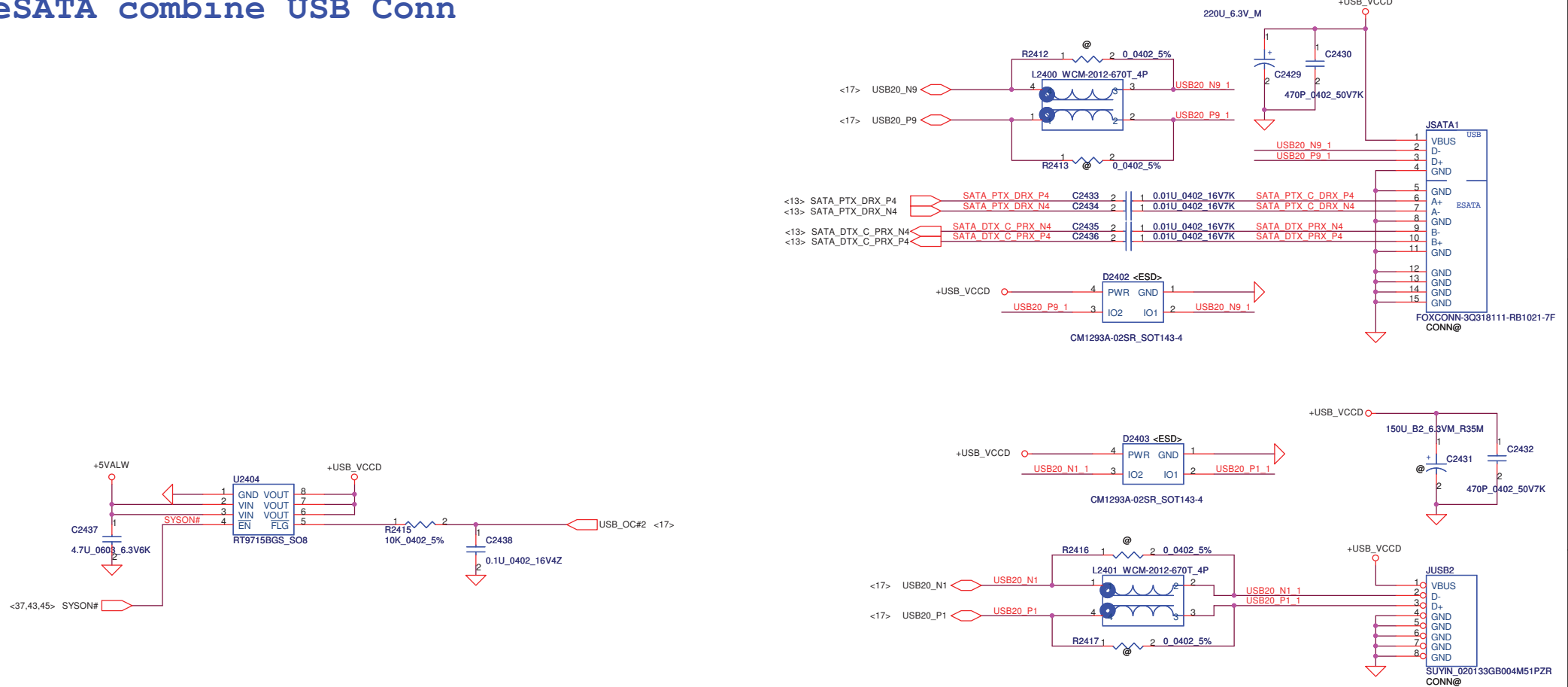


CIR



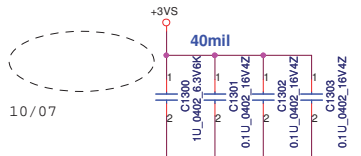
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eSATA combine USB Conn



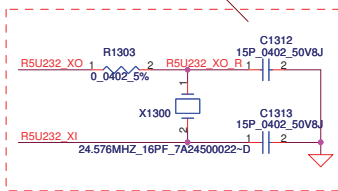
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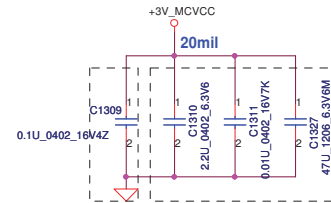


These caps close to U2 : Pin 12,37,48

Layout Note:
Place them close to U2

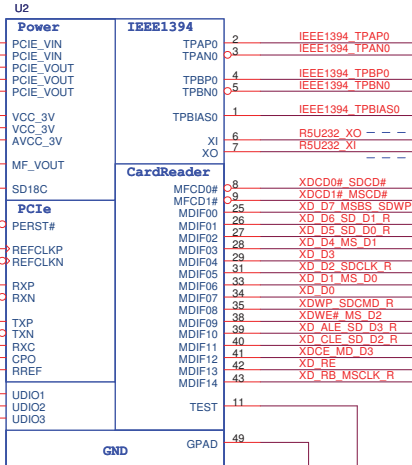
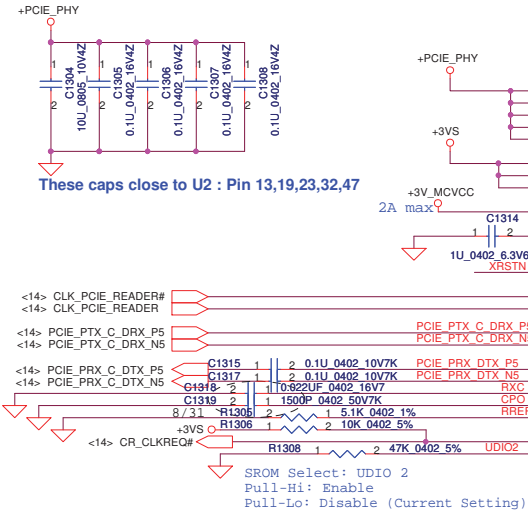


Memory Card Power



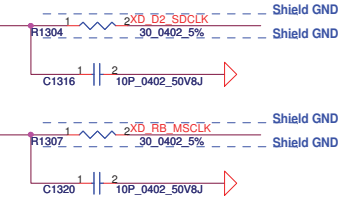
Layout Note:
Place them as close as possible to JREAD1
Place C1309 close to U2.36

These caps close to U2 : Pin 13,19,23,32,47

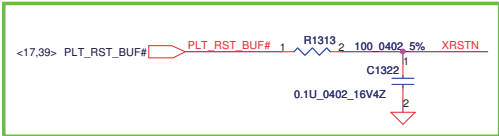
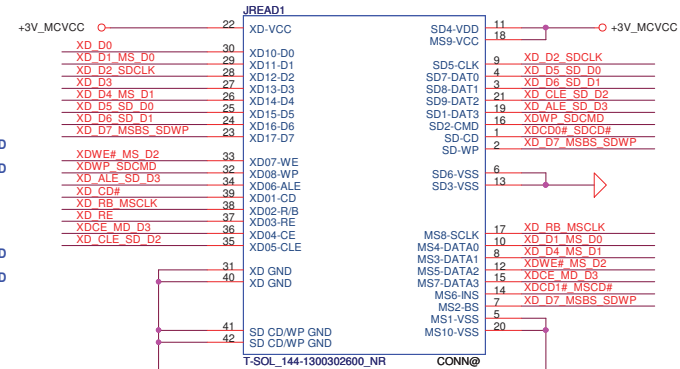


Layout Note:
Add GND shield for Xtal

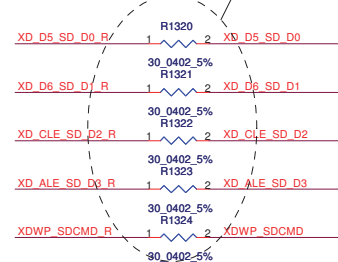
Impedance: 50 ohm (Microstrip)



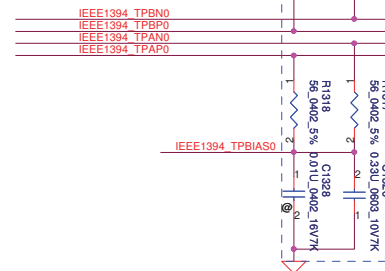
5 IN 1 CardRead



Layout Note:
Place them close to U2



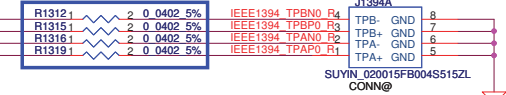
Layout Note:
Add GND shield for 1394.



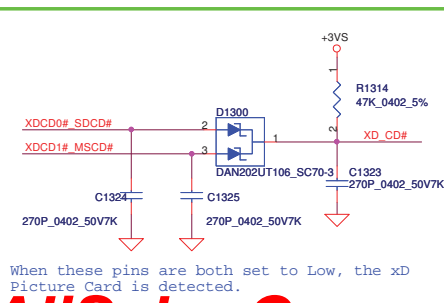
Layout Note:
Place them as close as possible to U2

Layout Note:
Place them as close as possible to JP1394
Reserve them for test
if any EMI issue.

Layout Note:
Differential pair impedance=110+/-6 Ohm
TPAP/N0 and TPBP/N0 mismatch <5mil



MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	-	D5
03	D7	D1	D4
04	D6	D5	D3
05	CLK	-	D2
06	-	D0	D1
07	D5	D4	D0
08	CMD	-	WP#
09	D4	D2	WE#
10	D3	D6	ALE
11	D2	-	CLE
12	-	D3	CE#
13	-	D7	RE#
14	CLK	RE#	-



When these pins are both set to Low, the xD Picture Card is detected.

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Compal Electronics, Inc.			
RSU232			
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The diagram illustrates the electrical connections for the ACES_88911-5204 CONN@ connector. Key components and connections include:

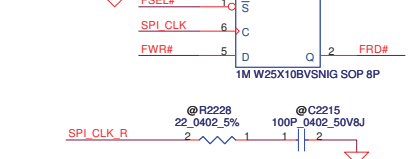
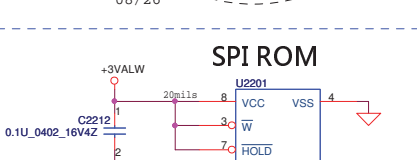
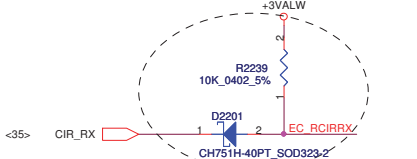
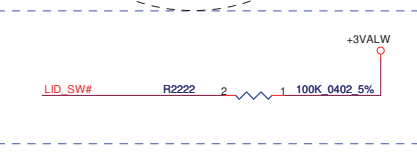
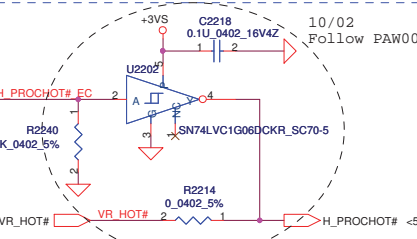
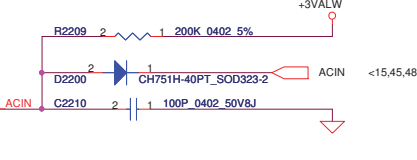
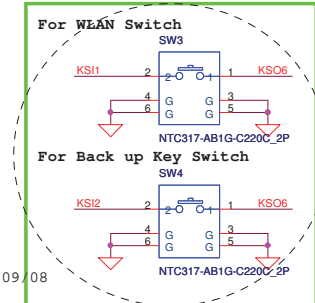
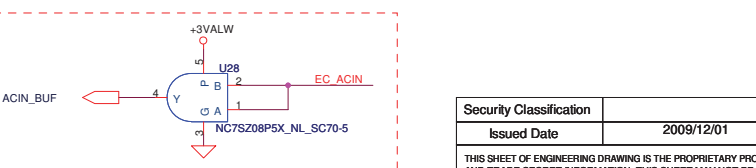
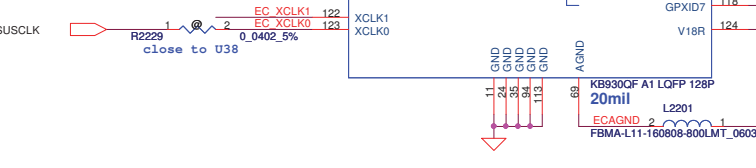
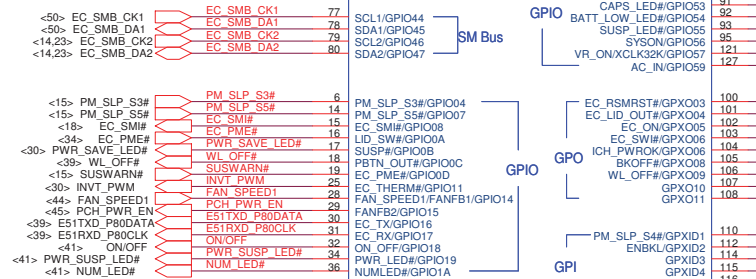
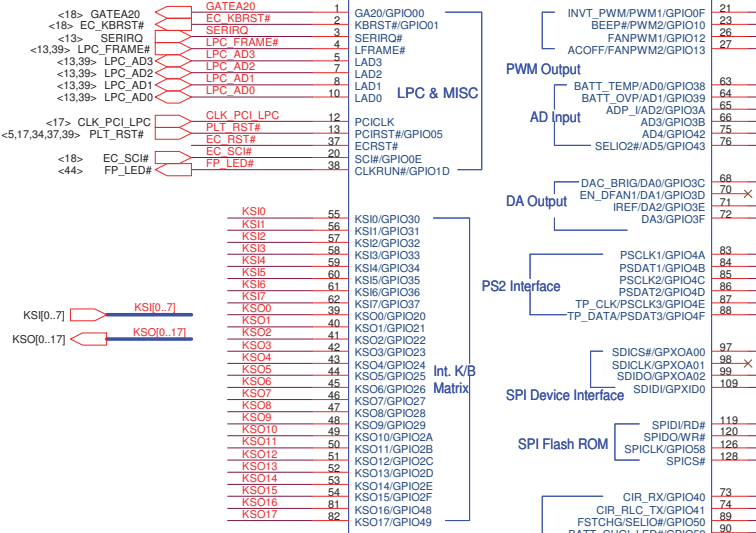
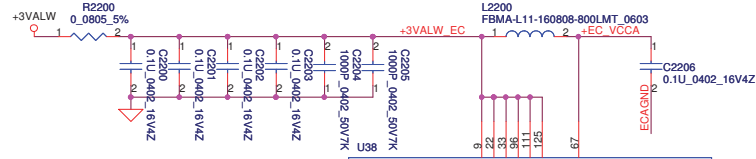
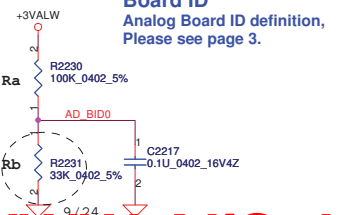
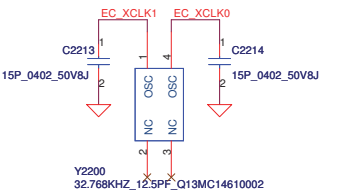
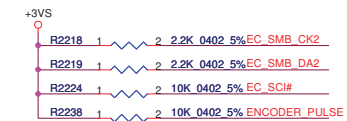
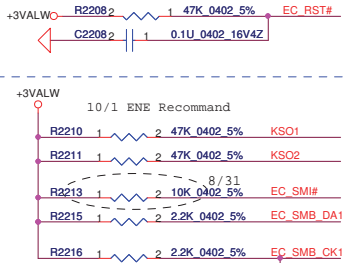
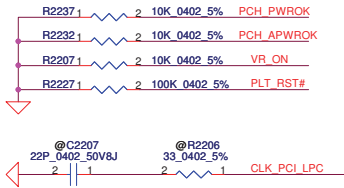
- Connector Pins:** 1 through 54, with specific functions assigned to each.
- Power Supply:** +3VS WLAN, +3VS, and +1.5VS.
- Resistors:** R2441 (2 0 0603 5%), R2442 (2 0 0603 5%), R2443 (2 0 0402 5%), R2444 (2 0 0402 5%), R2445 (10K 0402 5%), R2446 (100K 0402 5%).
- Capacitors:** C2476 (1 0.1uF), C2479 (1 0.1uF).
- Inductors:** L2476 (1 0.1uH), L2479 (1 0.1uH).
- Diodes:** D2476 (1 0.1uF), D2479 (1 0.1uF).
- Other Components:** R2448 (100K 0402 5%), R2449 (100K 0402 5%), R2450 (100K 0402 5%), R2451 (100K 0402 5%), R2452 (100K 0402 5%), R2453 (100K 0402 5%), R2454 (100K 0402 5%), R2455 (100K 0402 5%), R2456 (100K 0402 5%), R2457 (100K 0402 5%), R2458 (100K 0402 5%), R2459 (100K 0402 5%), R2460 (100K 0402 5%), R2461 (100K 0402 5%), R2462 (100K 0402 5%), R2463 (100K 0402 5%), R2464 (100K 0402 5%), R2465 (100K 0402 5%), R2466 (100K 0402 5%), R2467 (100K 0402 5%), R2468 (100K 0402 5%), R2469 (100K 0402 5%), R2470 (100K 0402 5%), R2471 (100K 0402 5%), R2472 (100K 0402 5%), R2473 (100K 0402 5%), R2474 (100K 0402 5%), R2475 (100K 0402 5%), R2476 (100K 0402 5%), R2477 (100K 0402 5%), R2478 (100K 0402 5%), R2479 (100K 0402 5%), R2480 (100K 0402 5%), R2481 (100K 0402 5%), R2482 (100K 0402 5%), R2483 (100K 0402 5%), R2484 (100K 0402 5%), R2485 (100K 0402 5%), R2486 (100K 0402 5%), R2487 (100K 0402 5%), R2488 (100K 0402 5%), R2489 (100K 0402 5%), R2490 (100K 0402 5%), R2491 (100K 0402 5%), R2492 (100K 0402 5%), R2493 (100K 0402 5%), R2494 (100K 0402 5%), R2495 (100K 0402 5%), R2496 (100K 0402 5%), R2497 (100K 0402 5%), R2498 (100K 0402 5%), R2499 (100K 0402 5%), R2500 (100K 0402 5%), R2501 (100K 0402 5%), R2502 (100K 0402 5%), R2503 (100K 0402 5%), R2504 (100K 0402 5%), R2505 (100K 0402 5%), R2506 (100K 0402 5%), R2507 (100K 0402 5%), R2508 (100K 0402 5%), R2509 (100K 0402 5%), R2510 (100K 0402 5%), R2511 (100K 0402 5%), R2512 (100K 0402 5%), R2513 (100K 0402 5%), R2514 (100K 0402 5%), R2515 (100K 0402 5%), R2516 (100K 0402 5%), R2517 (100K 0402 5%), R2518 (100K 0402 5%), R2519 (100K 0402 5%), R2520 (100K 0402 5%), R2521 (100K 0402 5%), R2522 (100K 0402 5%), R2523 (100K 0402 5%), R2524 (100K 0402 5%), R2525 (100K 0402 5%), R2526 (100K 0402 5%), R2527 (100K 0402 5%), R2528 (100K 0402 5%), R2529 (100K 0402 5%), R2530 (100K 0402 5%), R2531 (100K 0402 5%), R2532 (100K 0402 5%), R2533 (100K 0402 5%), R2534 (100K 0402 5%), R2535 (100K 0402 5%), R2536 (100K 0402 5%), R2537 (100K 0402 5%), R2538 (100K 0402 5%), R2539 (100K 0402 5%), R2540 (100K 0402 5%), R2541 (100K 0402 5%), R2542 (100K 0402 5%), R2543 (100K 0402 5%), R2544 (100K 0402 5%), R2545 (100K 0402 5%), R2546 (100K 0402 5%), R2547 (100K 0402 5%), R2548 (100K 0402 5%), R2549 (100K 0402 5%), R2550 (100K 0402 5%), R2551 (100K 0402 5%), R2552 (100K 0402 5%), R2553 (100K 0402 5%), R2554 (100K 0402 5%), R2555 (100K 0402 5%), R2556 (100K 0402 5%), R2557 (100K 0402 5%), R2558 (100K 0402 5%), R2559 (100K 0402 5%), R2560 (100K 0402 5%), R2561 (100K 0402 5%), R2562 (100K 0402 5%), R2563 (100K 0402 5%), R2564 (100K 0402 5%), R2565 (100K 0402 5%), R2566 (100K 0402 5%), R2567 (100K 0402 5%), R2568 (100K 0402 5%), R2569 (100K 0402 5%), R2570 (100K 0402 5%), R2571 (100K 0402 5%), R2572 (100K 0402 5%), R2573 (100K 0402 5%), R2574 (100K 0402 5%), R2575 (100K 0402 5%), R2576 (100K 0402 5%), R2577 (100K 0402 5%), R2578 (100K 0402 5%), R2579 (100K 0402 5%), R2580 (100K 0402 5%), R2581 (100K 0402 5%), R2582 (100K 0402 5%), R2583 (100K 0402 5%), R2584 (100K 0402 5%), R2585 (100K 0402 5%), R2586 (100K 0402 5%), R2587 (100K 0402 5%), R2588 (100K 0402 5%), R2589 (100K 0402 5%), R2590 (100K 0402 5%), R2591 (100K 0402 5%), R2592 (100K 0402 5%), R2593 (100K 0402 5%), R2594 (100K 0402 5%), R2595 (100K 0402 5%), R2596 (100K 0402 5%), R2597 (100K 0402 5%), R2598 (100K 0402 5%), R2599 (100K 0402 5%), R2600 (100K 0402 5%), R2601 (100K 0402 5%), R2602 (100K 0402 5%), R2603 (100K 0402 5%), R2604 (100K 0402 5%), R2605 (100K 0402 5%), R2606 (100K 0402 5%), R2607 (100K 0402 5%), R2608 (100K 0402 5%), R2609 (100K 0402 5%), R2610 (100K 0402 5%), R2611 (100K 0402 5%), R2612 (100K 0402 5%), R2613 (100K 0402 5%), R2614 (100K 0402 5%), R2615 (100K 0402 5%), R2616 (100K 0402 5%), R2617 (100K 0402 5%), R2618 (100K 0402 5%), R2619 (100K 0402 5%), R2620 (100K 0402 5%), R2621 (100K 0402 5%), R2622 (100K 0402 5%), R2623 (100K 0402 5%), R2624 (100K 0402 5%), R2625 (100K 0402 5%), R2626 (100K 0402 5%), R2627 (100K 0402 5%), R2628 (100K 0402 5%), R2629 (100K 0402 5%), R2630 (100K 0402 5%), R2631 (100K 0402 5%), R2632 (100K 0402 5%), R2633 (100K 0402 5%), R2634 (100K 0402 5%), R2635 (100K 0402 5%), R2636 (100K 0402 5%), R2637 (100K 0402 5%), R2638 (100K 0402 5%), R2639 (100K 0402 5%), R2640 (100K 0402 5%), R2641 (100K 0402 5%), R2642 (100K 0402 5%), R2643 (100K 0402 5%), R2644 (100K 0402 5%), R2645 (100K 0402 5%), R2646 (100K 0402 5%), R2647 (100K 0402 5%), R2648 (100K 0402 5%), R2649 (100K 0402 5%), R2650 (100K 0402 5%), R2651 (100K 0402 5%), R2652 (100K 0402 5%), R2653 (100K 0402 5%), R2654 (10

The diagram illustrates the electrical connection between the ACES_88915-5204 module and the USB20 module. The module's pin headers are JMINI2 (pins 1-53) and CONN@ (pins 1-54). The USB20 module's pins are labeled with their functions: WAKE#, RESERVED, CLKREQ#, REFCLK-, REFCLK+, GND, PER#0, PER#0, GND, SMB_CLK, SMB_DATA, USB_D-, USB_D+, LED_WWAN#, LED_WLAN#, LED_WLAN#, RESERVED, +1.5V, +3.3V, and GND. The connections are as follows:

- Power Connections:**
 - +3VS_TV:** Connected to pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53, and 54.
 - +3VS:** Connected to pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, and 52.
- Signal Connections:**
 - PCH_PCIE_WAKE#:** Connected to pin 1.
 - WAKE#:** Connected to pin 2.
 - CLKREQ#:** Connected to pin 3.
 - REFCLK-:** Connected to pin 4.
 - REFCLK+:** Connected to pin 5.
 - GND:** Connected to pins 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, and 54.
 - PER#0:** Connected to pins 25 and 27.
 - SMB_CLK:** Connected to pin 30.
 - SMB_DATA:** Connected to pin 32.
 - USB_D-:** Connected to pin 36.
 - USB_D+:** Connected to pin 38.
 - LED_WWAN#:** Connected to pin 42.
 - LED_WLAN#:** Connected to pin 44.
 - LED_WLAN#:** Connected to pin 46.
 - RESERVED:** Connected to pins 48, 50, and 52.
 - +1.5V:** Connected to pin 50.
 - +3.3V:** Connected to pin 52.
- Other Connections:**
 - PLT_RST_BUF#:** Connected to pin 22.
 - D CK SCLK:** Connected to pin 28.
 - D CK SDATA:** Connected to pin 30.
 - USB20_N5 <17>:** Connected to pin 34.
 - USB20_P5 <17>:** Connected to pin 36.

The diagram also shows the module's dimensions (H=5.2mm) and the part number (ACES_88915-5204).

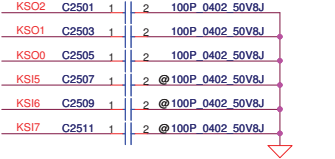
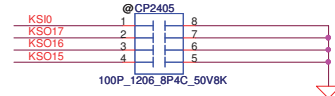
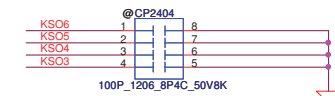
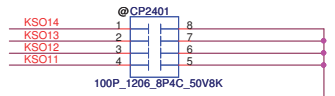
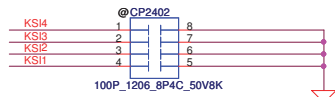
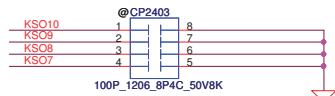
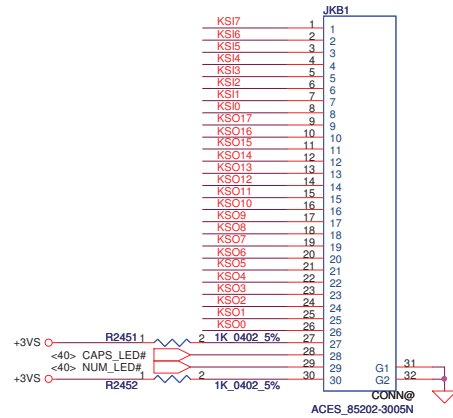
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				Document Number LA-6931P	
				Date: Wednesday, October 27, 2010	Sheet 39 of 58



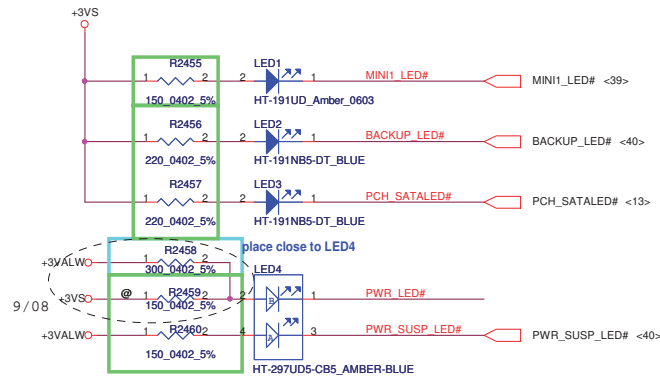
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Issued Date	2009/12/01	Deciphered Date	2010/12/31																
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<table border="1"> <tr> <th colspan="2">Title</th><th colspan="2">Compal Electronics, Inc.</th></tr> <tr> <td colspan="2">EC ENCE-KB930</td><td colspan="2">Document Number</td></tr> <tr> <td colspan="2">LA-6931P</td><td colspan="2">Rev</td></tr> <tr> <td colspan="2">Date: Wednesday, October 27, 2010</td><td colspan="2">Sheet 40 of 58</td></tr> </table>				Title		Compal Electronics, Inc.		EC ENCE-KB930		Document Number		LA-6931P		Rev		Date: Wednesday, October 27, 2010		Sheet 40 of 58	
Title		Compal Electronics, Inc.																	
EC ENCE-KB930		Document Number																	
LA-6931P		Rev																	
Date: Wednesday, October 27, 2010		Sheet 40 of 58																	

INT_KBD Conn.

KSIO[0..7] <40>
KSIO[0..17] <40>

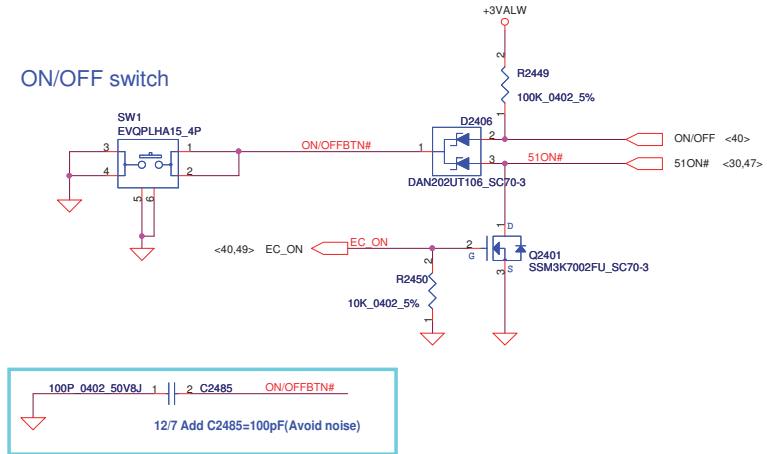


LED

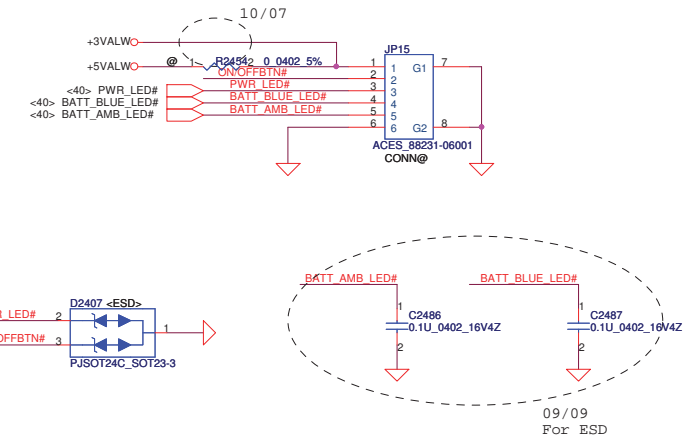


Power Button

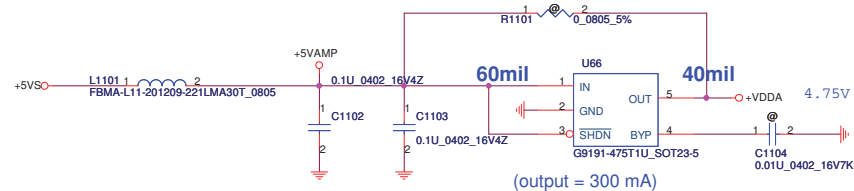
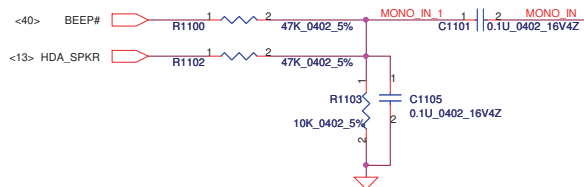
ON/OFF switch



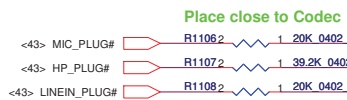
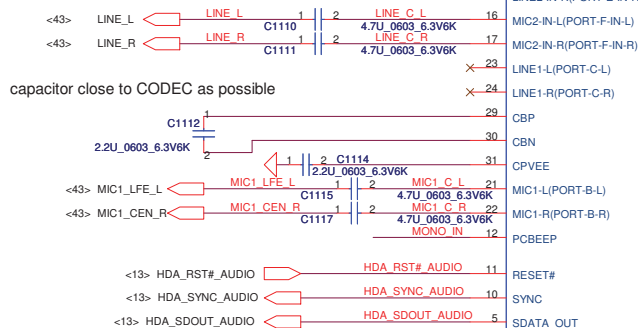
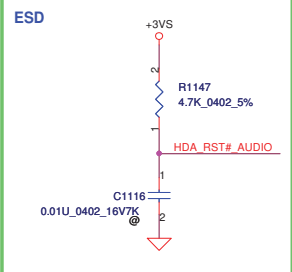
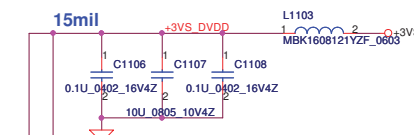
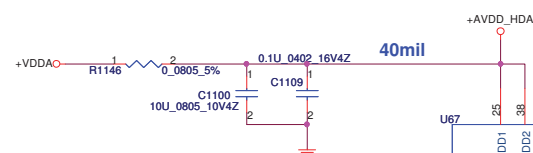
Power Conn



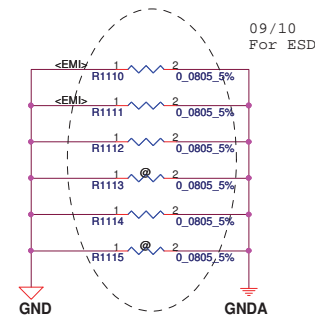
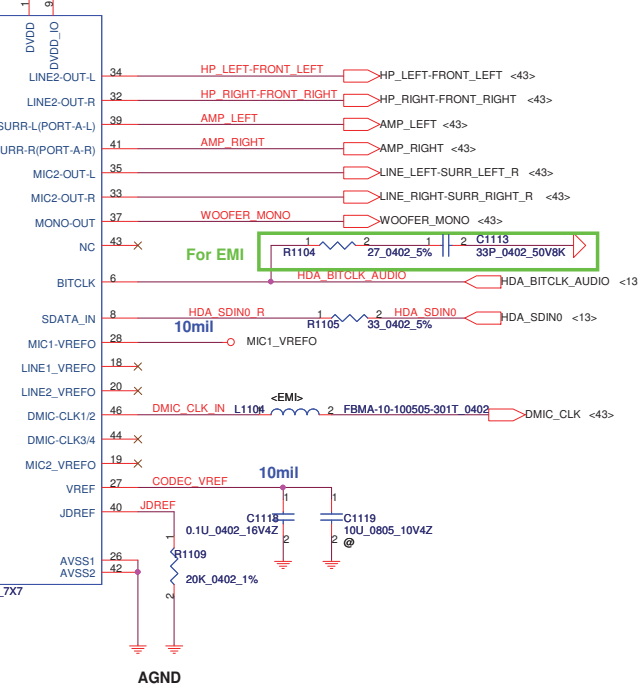
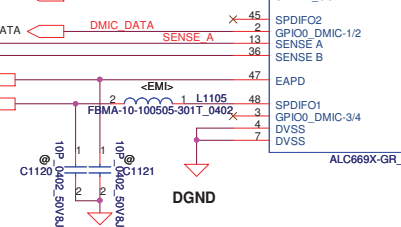
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Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title Power OK, I/O Port & K/B Connector		
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HD Audio Codec



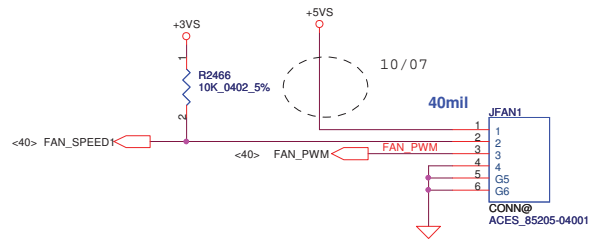
Sense Pin	Impedance	Codec Signals
SENSE A	20K	PORT-A (PIN 39, 41)
		PORT-B (PIN 21, 22)
		PORT-C (PIN 23, 24)
SENSE B	39.2K	PORT-E (PIN 32, 34)
	20K	PORT-F (PIN 33, 35)
		PORT-H (PIN 37)



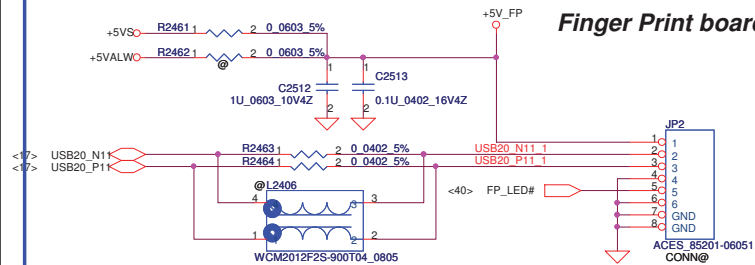
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				Date: Wednesday, October 27, 2010	Sheet 42 of 58

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				Custom	LA-6931P	1.0
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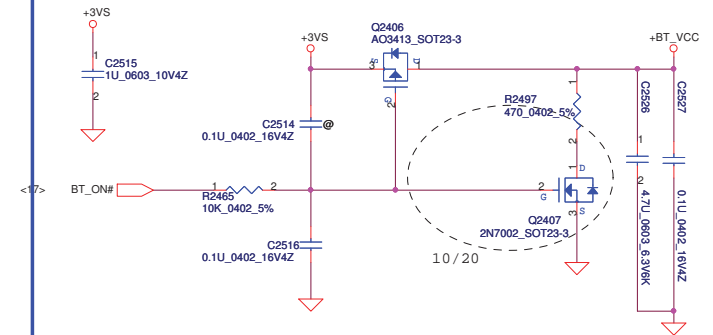
FAN1 Conn



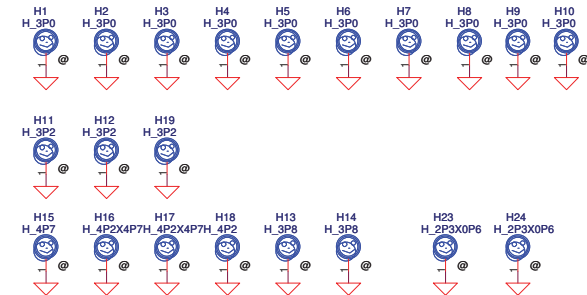
Finger Print board



BT



Screw



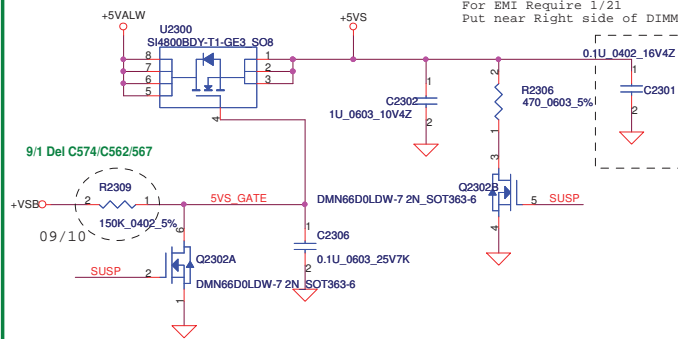
NON-PDH

2/25 Change footprint of H22

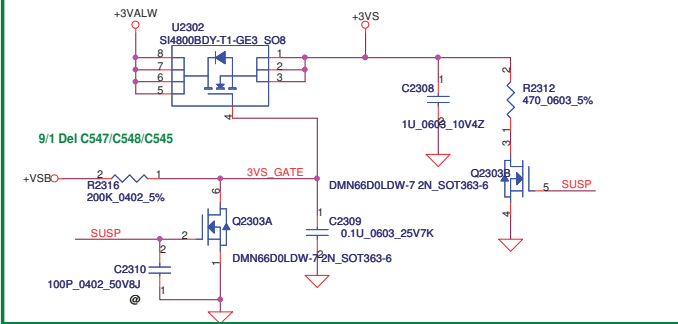


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+5VALW TO +5VS

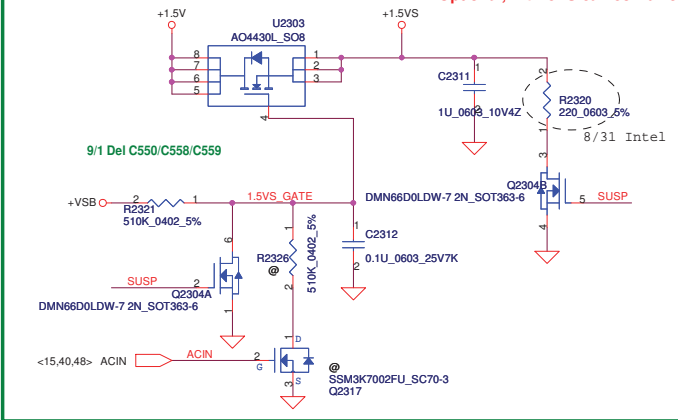


+3VALW TO +3VS

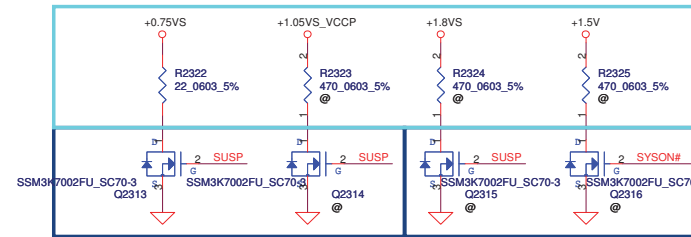
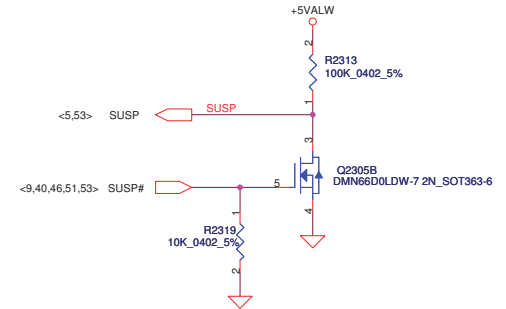
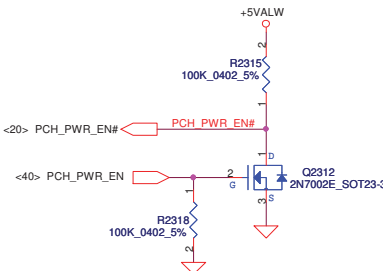
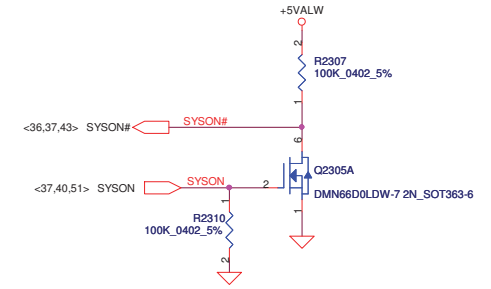
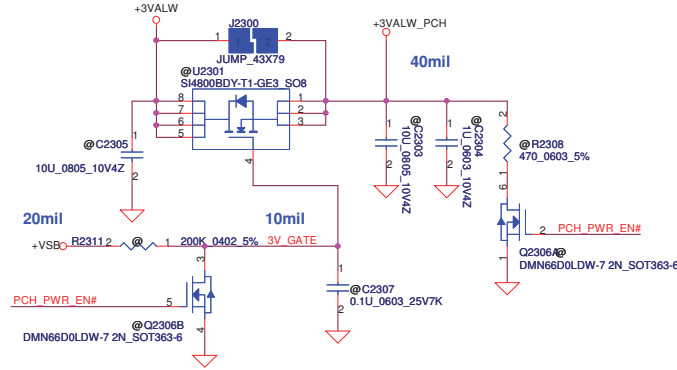


+1.5V to +1.5VS

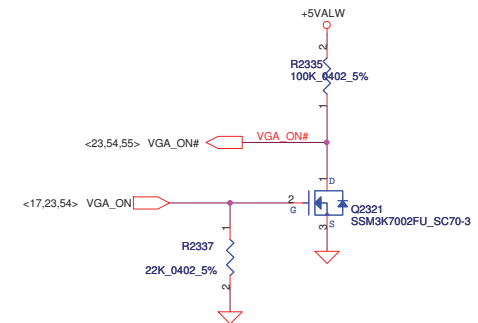
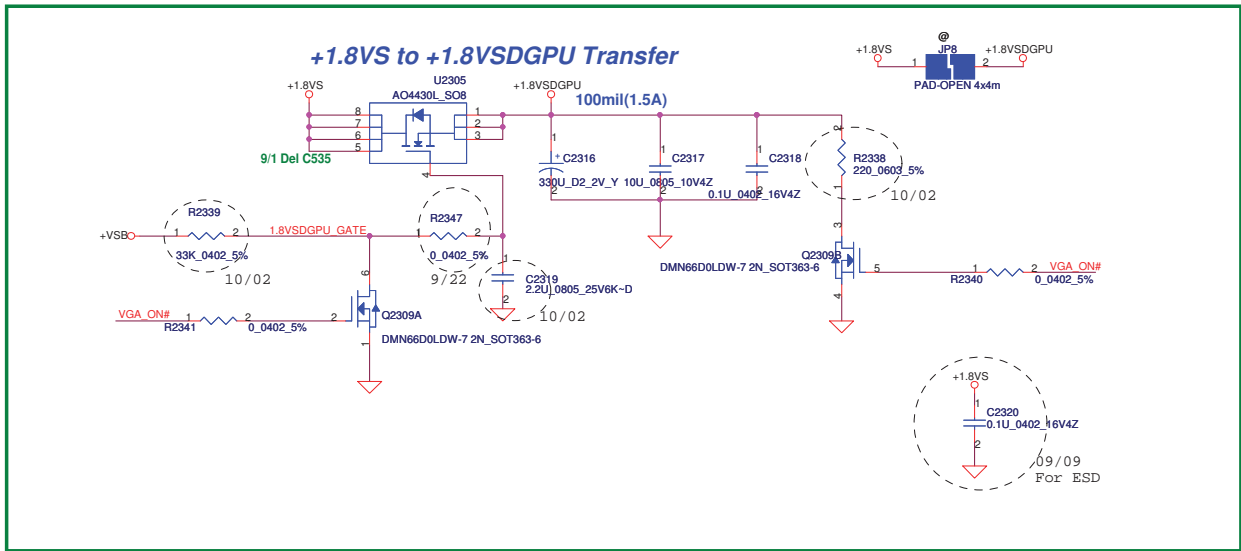
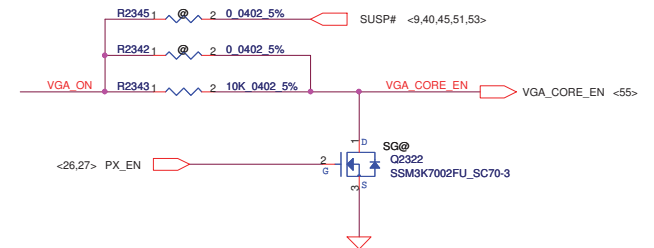
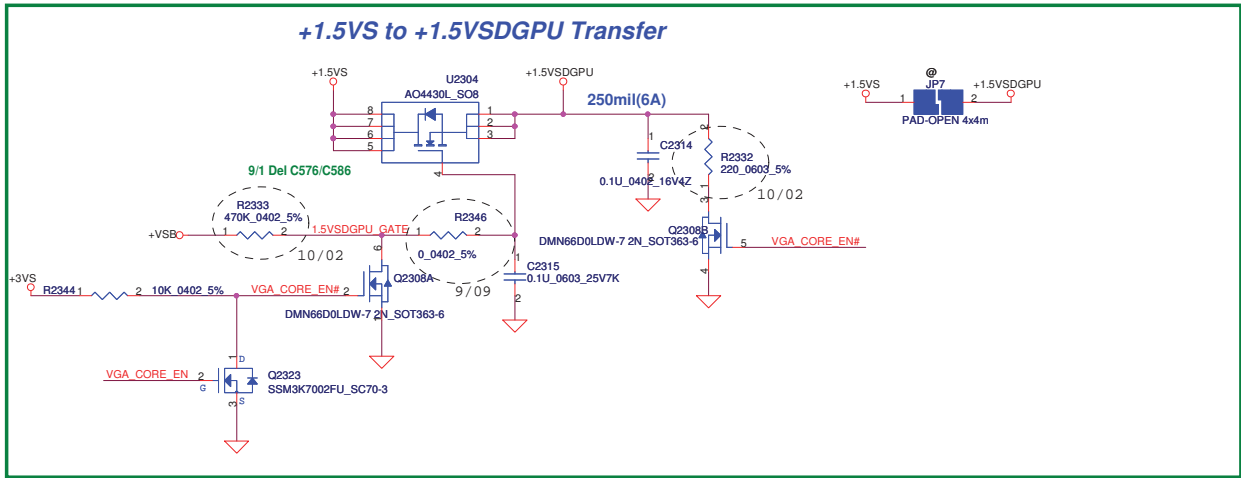
Optional, if +1.5VS can combine with +1.5V_1



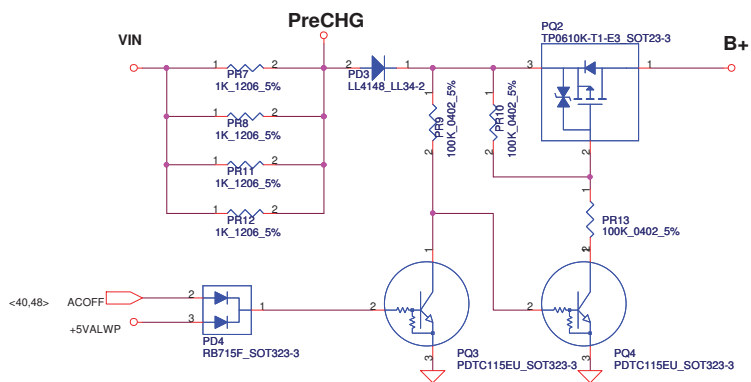
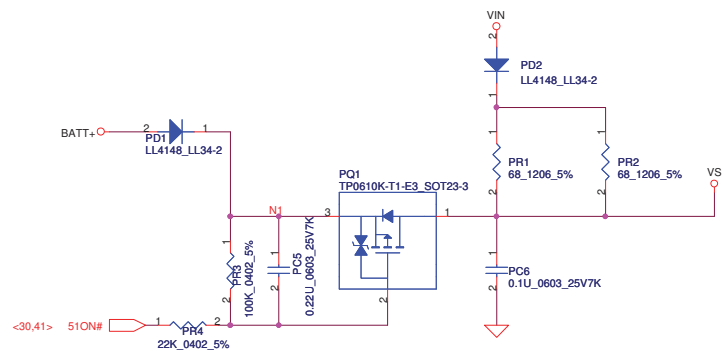
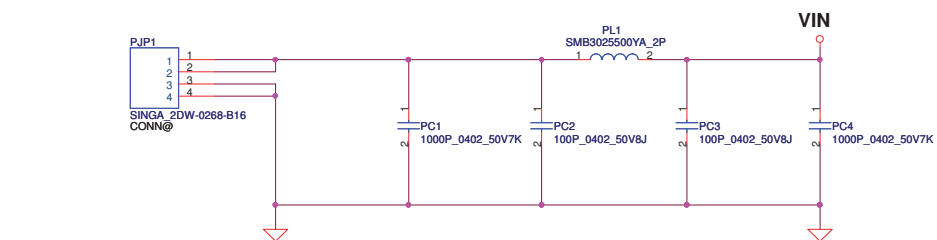
+3VALW TO +3VALW(PCH AUX Power) Short J5 for PCH VCCSUS3.3



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						B	LA-6931P		1.0	
						Date:	Wednesday, October 27, 2010		Sheet 45 of 58	



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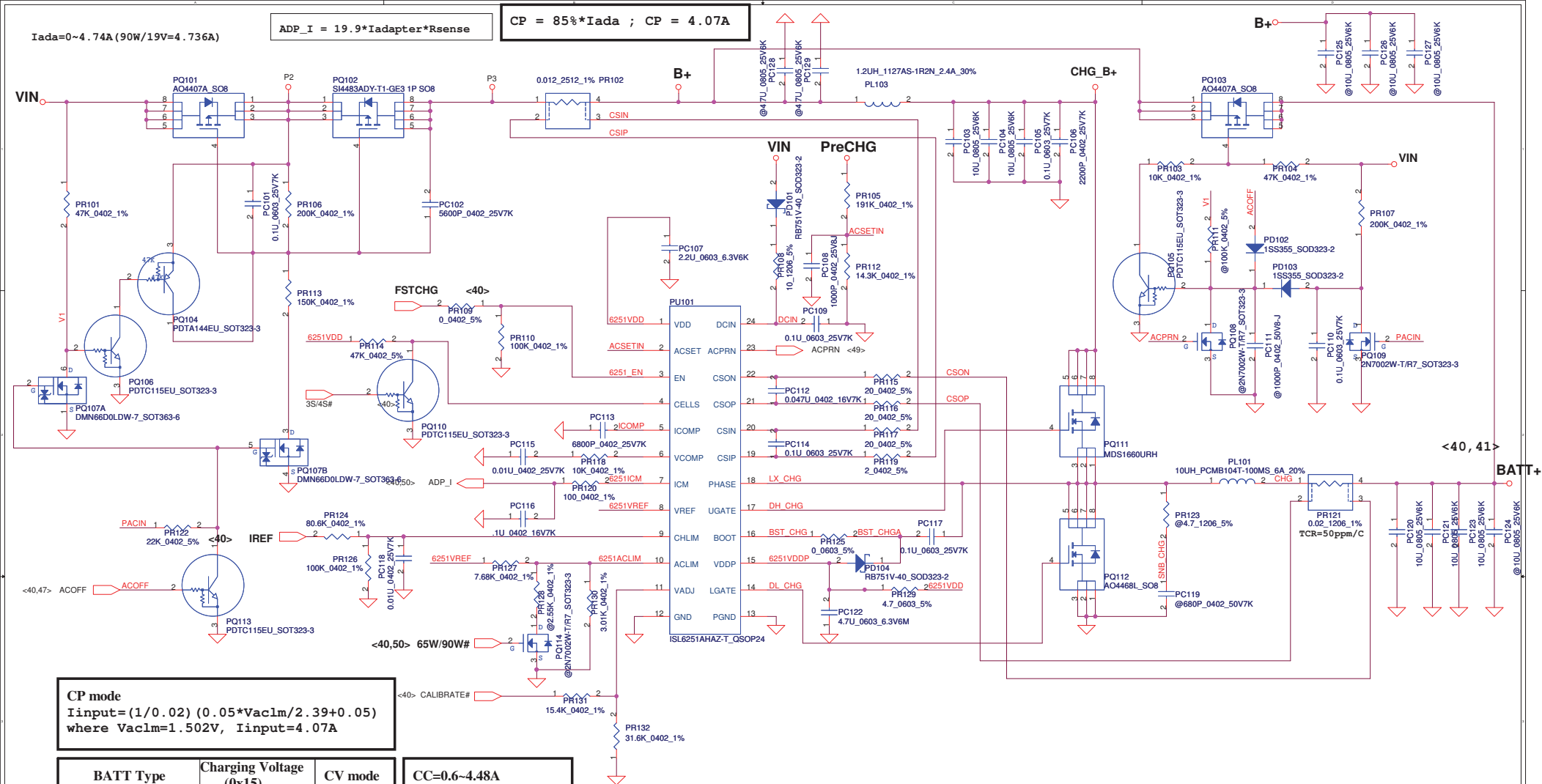


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Iada=0~4.74A (90W/19V=4.736A)

ADP_I = 19.9*Iadaprer*Rsense

CP = 85%*Iada ; CP = 4.07A

**CP mode**

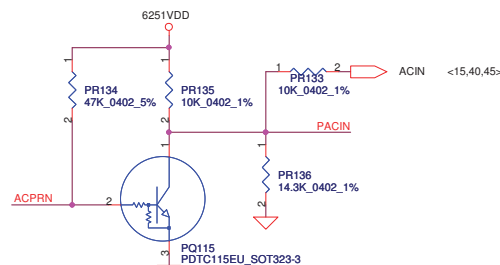
$I_{input} = (1/0.02) (0.05 \cdot V_{acim}/2.39 + 0.05)$
 where $V_{acim} = 1.502V$, $I_{input} = 4.07A$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

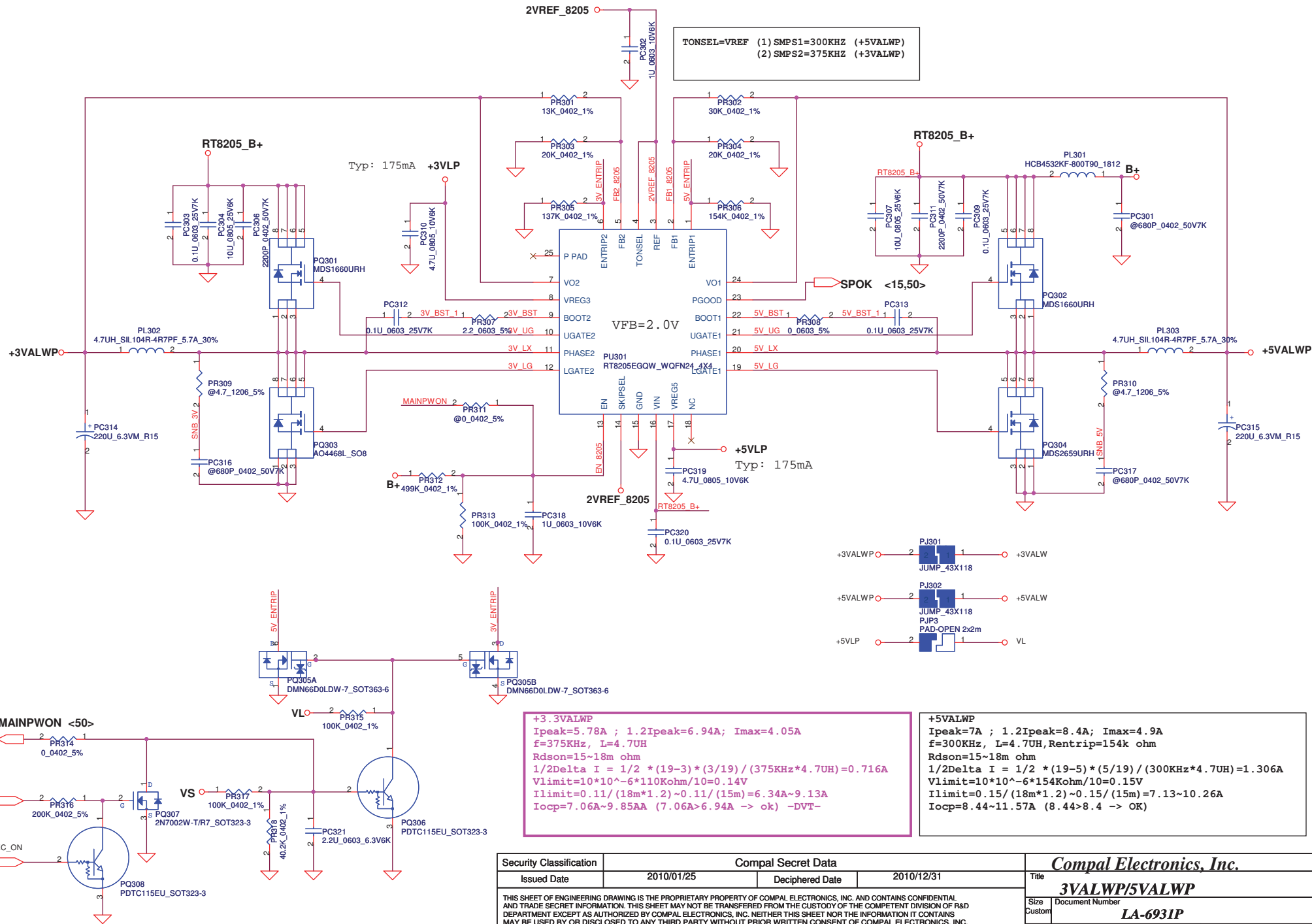
CC=0.6~4.48A
IREF=0.7224*Icharge
IREF=0.43V~3.24V

Ki
 $V_{chlim} = I_{ref} \cdot (PR374 / (PR372 + PR374))$
 $= I_{ref} \cdot (100K / (80.6K + 100K))$
 $= I_{ref} \cdot 0.5537$
 $I_{charge} = (165mV / PR369) \cdot (V_{chlim} / 3.3V)$
 $= (165mV / 20m) \cdot (1/3.3V) \cdot I_{ref} \cdot 0.5537$
 $= 1.3842 \cdot I_{ref}$
 $I_{ref} = 0.7224 \cdot I_{charge} \Rightarrow Ki = 0.7224$

Kv
 $R_{internal} = ic = 514K$ $R_{ec} = 3K$ $R1 = PR379 = 15.4K$ $R2 = PR381 = 31.6K$
 $R = 514K // 31.6K // (15.4K + 3K) = 11.372K$
 $r = 514K // 514K // 31.6K = 28.14K$
 $V_{cell} = 0.175 \cdot V_{adj} + 3.99V$
 $4.2V = 0.175 \cdot V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} \cdot (R / (R + 514K)) + CALIBRATE \cdot (r / (r + 514K))$
 $1.1483 = CALIBRATE \cdot 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell} + A \cdot 0.175)) \cdot Kv = (4.2 - (4.2 + A \cdot 0.175)) \cdot Kv$
 $A = V_{ref} \cdot (R / (R + 514K)) = 0.052$
 $Kv = 9.451$

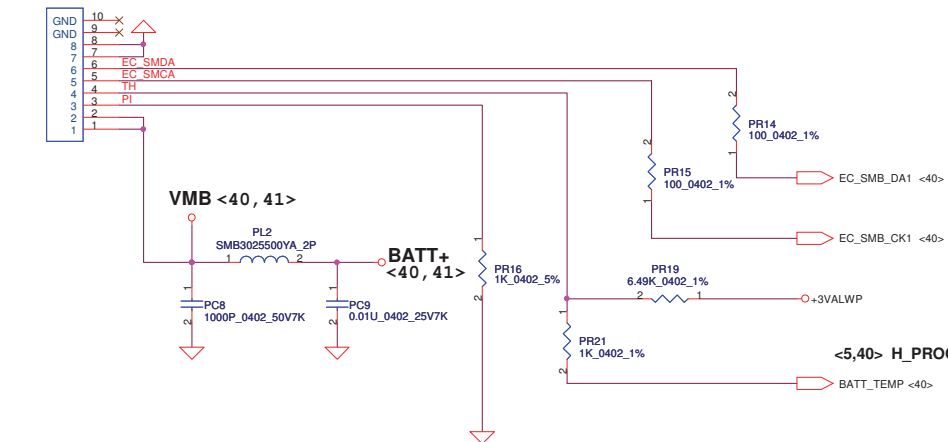


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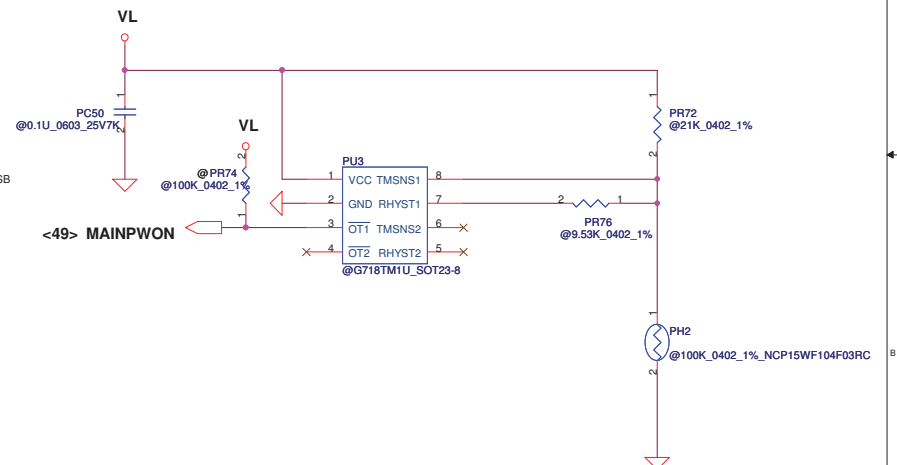
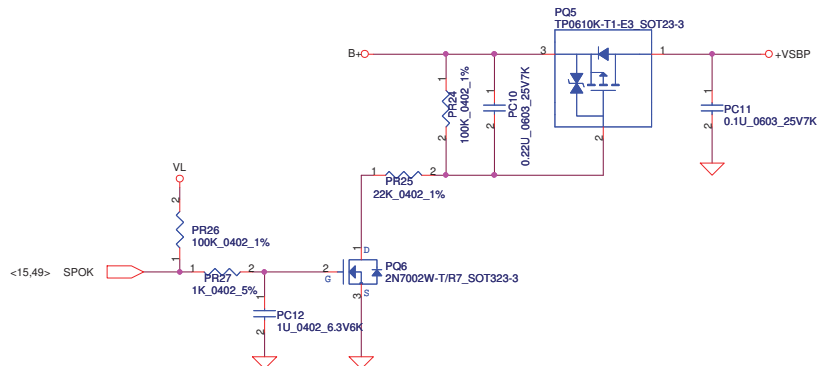
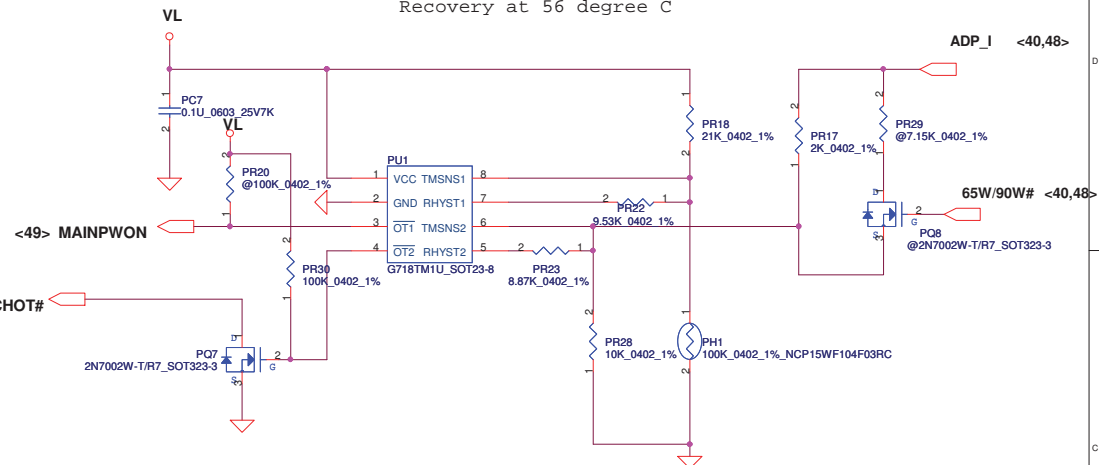


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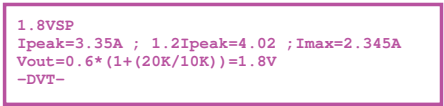
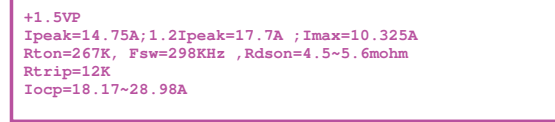
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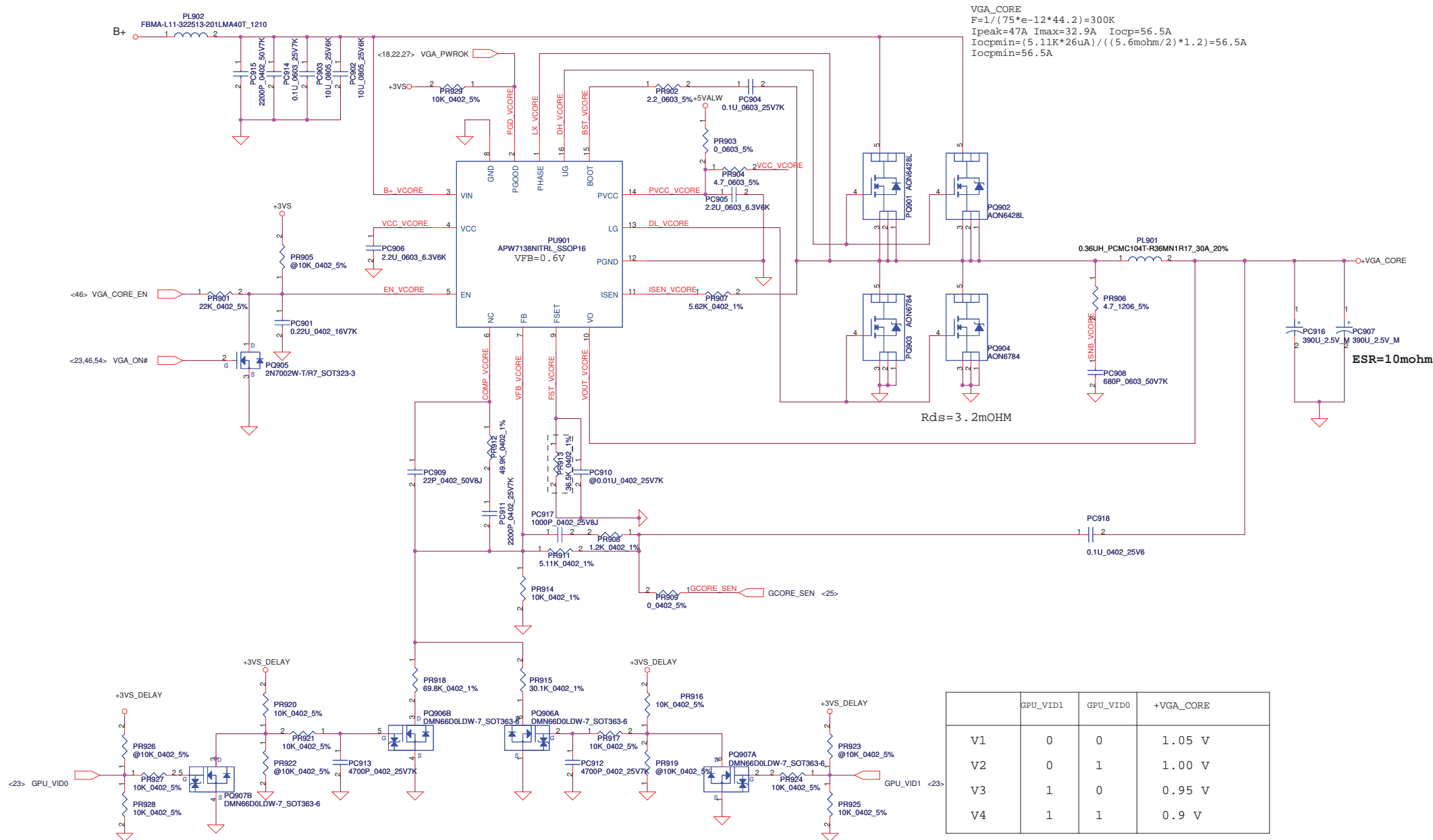
PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



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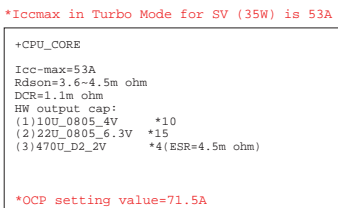


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Parallel and tune length



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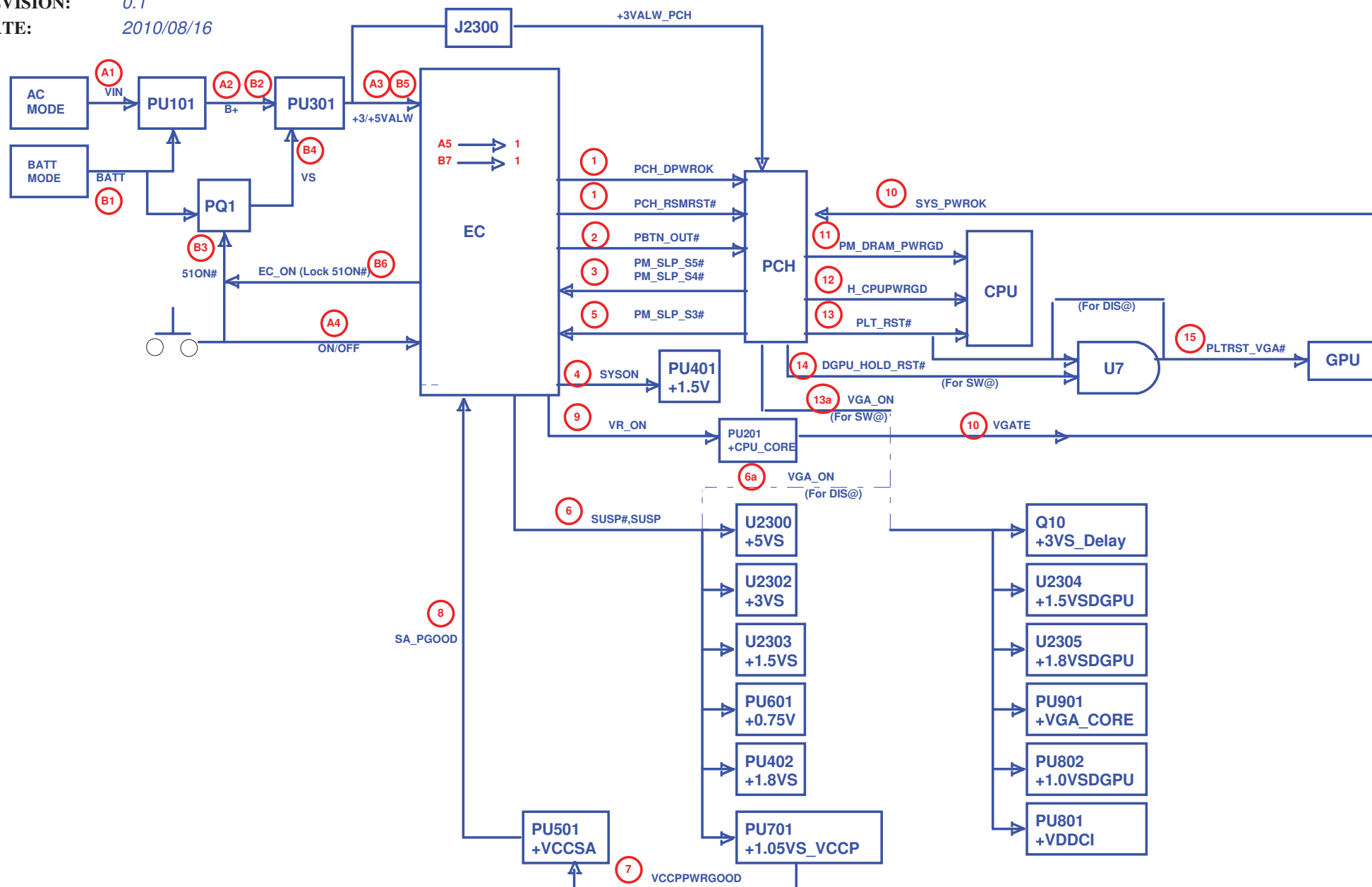
COMPAL CONFIDENTIAL

MODEL NAME: P5LM0 Power Sequence Block Diagram

PCB NAME: LA-6931P

REVISION: 0.1

DATE: 2010/08/16



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